QuickLogic® PolarPro® 3E Device Data Sheet

Low Power FPGA Combining Efficient Logic Cells with Embedded RAM and FIFO Blocks to Maximize Logic Density in Minimal PCB Space

Device Highlights

Low Power

- 145 µA static power consumption, suitable for smartphones, tablets, mobile enterprise devices and other power sensitive applications
- Prolongs device battery life

Small Form Factor Packaging

- 3,500 effective logic cells
- 2.19 mm x 2.47 mm WLCSP
- 3.5 mm x 3.5 mm VFBGA
- Designed for the most space-sensitive applications

Complete Customizable Solutions

- Allows offloading of computationally intensive applications
- Includes comprehensive software packages along with hardware

Efficient Logic Utilization

- Flexible logic cells, capable of two independent 3-input LUTs or a single 4-input LUT.
- Allows greater functionality in less PCB space

Embedded Standard Blocks

- Built in SRAM and FIFO controllers, I^2C Master, and SPI Slave interfaces
- Dual 32 x 32 multipliers
- Enables data buffering and autonomous data transfers

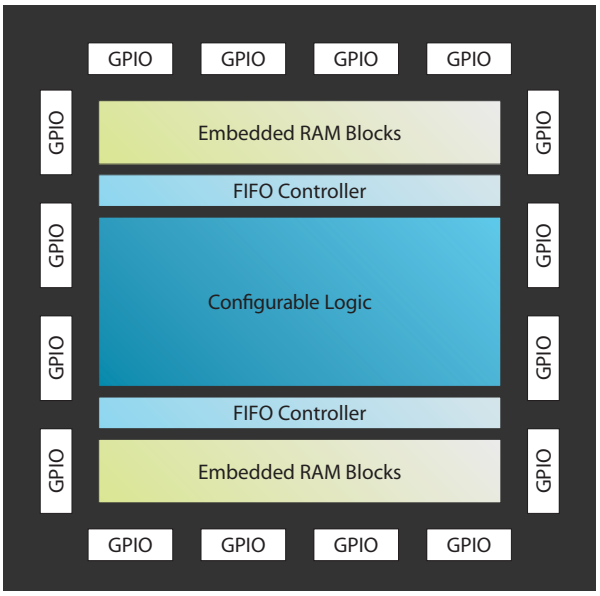
Fast Time-to-Market

- QuickLogic designs and delivers complete Customer Specific Standard Product (CSSP) solutions, including hardware and software
- Uses QuickLogic's existing library of Proven System Blocks (PSBs)
- Reduces development time and costs

Flexible Reconfigurable Logic

- 1.2 V core voltage, 1.8/2.5/3.3 V drive capable I/Os
- 145 µA standby current
- Up to 46 I/Os available
- Up to 3,500 effective logic cells
- Reconfigurable SRAM technology

Figure 1: PolarPro 3E Block Diagram



Embedded Dual-Port SRAM

- Up to eight dual-port 8-kilobit high performance SRAM blocks
- True dual-port capability
- Embedded synchronous/asynchronous FIFO controllers
- Configurable and cascadable aspect ratio

16 KB SRAM Block

- 8 KB
- 2X 512 x 36 memories
- 2X 512 x 32 memories

Configurable I/O

- Configurable dual drive strength per GPIO
- Independent I/O banks capable of supporting multiple I/O standards in one device
- Bank programmable I/O standards: LVTTL, LVCMOS25 and LVCMOS18
- Weak pull-down and pull-up capability and input enables
- 2X drive-configurable I/O

Advanced Clock Network

- Multiple low skew clock networks
  - 5 programmable global clock networks
- Quadrant-based segmentable clock networks
  - 20 quad clock networks per device

Hardened IP

- I^2C Master
- SPI Slave
- High speed oscillator
- LED driver
- 32 x 32 multiplier (2X)

Introduction

PolarPro 3E was specifically architected to meet the increasingly complex needs of mobile device OEMs. With special attention paid to efficient logic cell utilization, smallest size, and lowest power consumption during the design process, PolarPro 3E is the ideal solution for OEMs who require a configurable logic solution for their application. PolarPro 3E operates seamlessly with any processor available on the market today to address emerging connectivity, sensor control, and custom applications. QuickLogic combines PSBs and software drivers, along with customer-specific logic, to deliver CSSPs based on the exact requirements of our customers.

Table 1 summarizes the PolarPro 3E device family features.

Table 1: PolarPro 3E Device Family

Features		PolarPro 3E
Max Gates		175,000
Effective Logic Cells		3,500
8K RAM Modules (9216 bits)		8
FIFO Controllers		8
RAM bits		73,728 bits (fabric) + [65,536 + 36,864 + 32,768] bits Application-Specific Standard Product (ASSP)
Max I/O per Package	30-ball WLCSP (0.4 mm pitch)	18
	64-ball VFBGA (0.4 mm pitch)	46

Programmable Logic Architectural Overview

The QuickLogic PolarPro 3E logic cell structure presented in **Figure 2** is a single register, multiplexer-based logic cell. It is designed for wide fan-in and multiple, simultaneous output functions. The cell has a high fan-in, fits a wide range of functions with up to 22 simultaneous inputs (including register control lines), and four outputs (three combinatorial and one registered). The high logic capacity and fan-in of the logic cell accommodates many user functions with a single level of logic delay.

The PolarPro 3E logic cell can implement:

- Two independent 3-input functions
- Any 4-input function
- 8 to 1 mux function
- Independent 2 to 1 mux function
- Inverted or non-inverted clock signal to flip-flop
- Single dedicated register with active high clock enable, set and reset signals
- Direct input selection to the register, which allows combinatorial and register logic to be used separately
- Combinatorial logic can also be configured as an edge-triggered master-slave D flip-flop

Figure 2: PolarPro 3E Logic Cell

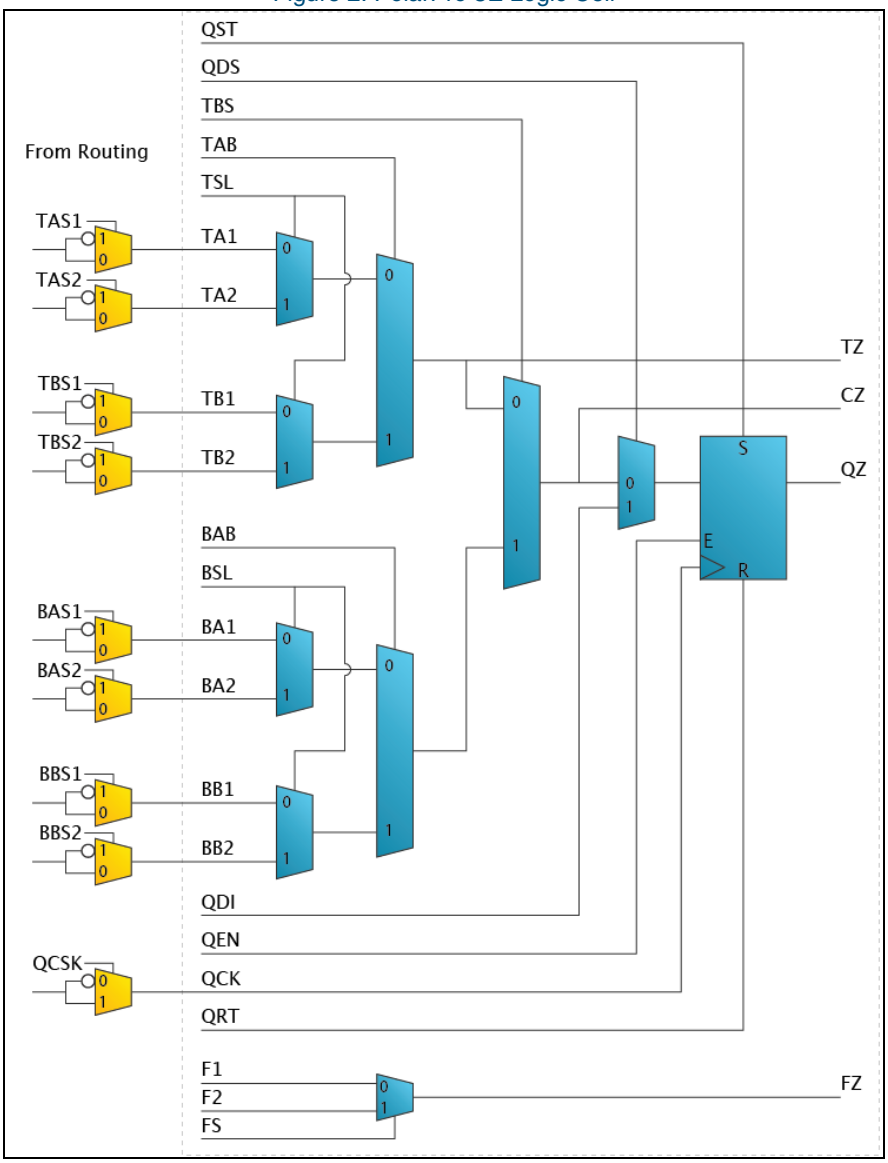


Table 2 describes the PolarPro 3E logic cell functions that are shown in **Figure 2**.

Table 2: PolarPro 3E Logic Cell Functions

Name	Function	Type	Description
QDS	Input	Control	Mux Select
TBS	Input	Control	Mux Select
TAB	Input	Control	Mux Select
TSL	Input	Control	Mux Select
TA1	Input	Data Signal	Mux Inputs
TB1	Input	Data Signal	Mux Inputs
TB2	Input	Data Signal	Mux Inputs
BAB	Input	Data Signal	Mux Inputs
BSL	Input	Data Signal	Mux Inputs
BA1	Input	Data Signal	Mux Inputs
BA2	Input	Data Signal	Mux Inputs
BB1	Input	Data Signal	Mux Inputs
BB2	Input	Data Signal	Mux Inputs
QDI	Input	Data Signal	Mux Inputs
QEN	Input	Control	SR REG ENABLE
QCK	Input	Clock Signal	SR REG CLK
QRT	Input	Control	SR REG RESET
F1	Input	Data Signal	Mux Inputs
F2	Input	Data Signal	Mux Inputs
FS	Input	Control	Mux Select
TZ	Output	Data Signal	Mux Output
CZ	Output	Data Signal	Mux Output
QZ	Output	Data Signal	SR REG OUT
FZ	Output	Data Signal	Mux Output
F1	Input	Data Signal	Mux Inputs
F2	Input	Data Signal	Mux Inputs

Effective Logic Cells

The PolarPro 3E family features the unique ability to implement two independent 3-input look-up tables (LUT) or a single 4-input LUT from a single logic cell. Typical programmable fabric logic cells only contain a single 4-input LUT, which significantly impairs the ability of the FPGA designer to create space-efficient implementations. The PolarPro 3E logic architecture enables much higher utilization designs, whether through more functions in the same number of logic cells or identical functions in significantly less logic cells.

Effective logic cells represent a metric that fairly compares the utilization of QuickLogic's flexible LUT design versus standard single LUT FPGA designs.

RAM Modules

The PolarPro 3E family of devices includes up to eight 8 kilobits (9,216 bits) dual-port RAM modules for implementing RAM and FIFO functions.

RAM features include:

- Independently configurable read and write data bus widths
- Independent read and write clocks
- Inverted or non-inverted clock signals to read and write clock inputs
- Horizontal and vertical concatenation
- Write byte enables
- Selectable pipelined or non-pipelined read data

Figure 3 shows the 8-kilobit Dual-Port RAM block.

Figure 3: 8-Kilobit Dual-Port RAM Block 512 x 18 Configuration

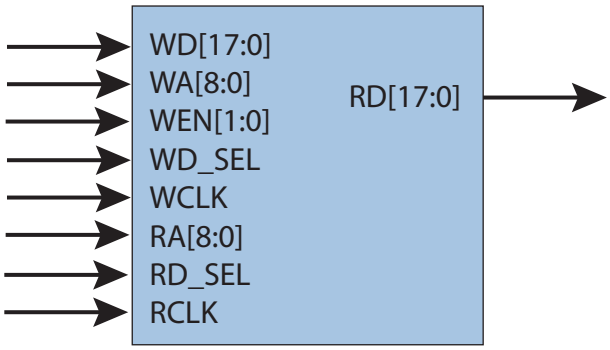


Table 3 describes the RAM interface signals.

Table 3: RAM Interface Signals

Signal Name	Function
Inputs	
WD [17:0]	Write Data
WA [8:0]	Write Address
WEN [1:0]	Write Enable (two 9-bit enables)
WD_SEL	Write Chip Select
WCLK	Write Clock
RA [8:0]	Read Address
RD_SEL	Read Chip Select
RCLK	Read Clock
Output	
RD [17:0]	Read Data Output

Table 4 describes the ASSP RAM interface signals.

Table 4: ASSP RAM Interface Signals

Signal Name	Function
Inputs	
RAM_ADDR [8:0]	Write Address
RAM_WR_DATA [35:0]	Write Data
RAM_RD_EN	Read Enable
RAM_WR_EN	Write Enable
RAM_WR_BE [3:0}	Byte Enable
RAM_ADDR [8:0]	Write Address
Output	
RAM_RD_DATA [35:0]	Read Data

The read and write data buses of a RAM block can be arranged to variable bus widths. The bus widths can be configured using the RAM Wizard available in QuickWorks, QuickLogic's development software. The selection of the RAM depth and width determines how the data is addressed.

The RAM blocks also support data concatenation. Designers can cascade multiple RAM modules to increase the depth or width by connecting corresponding address lines together and dividing the words between modules. Generally, this requires the use of additional programmable logic resources. However, when concatenating only two 8-kilobit RAM blocks, they can be concatenated horizontally or vertically without using any additional programmable fabric resources.

For example, two internal dual-port RAM blocks can be concatenated vertically to create a 1024x18 RAM block or horizontally to create a 512x36 RAM block. A block diagram of horizontal and vertical concatenation is displayed in **Figure 4**.

Figure 4: Horizontal and Vertical Concatenation Examples

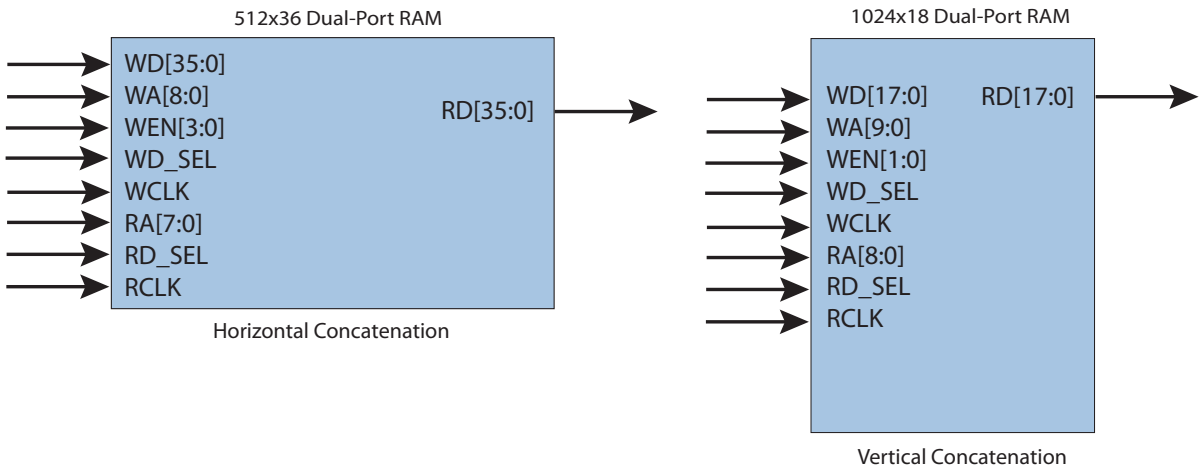


Table 5 shows the various configurations supported by the PolarPro 3E 8-kilobit RAM modules.

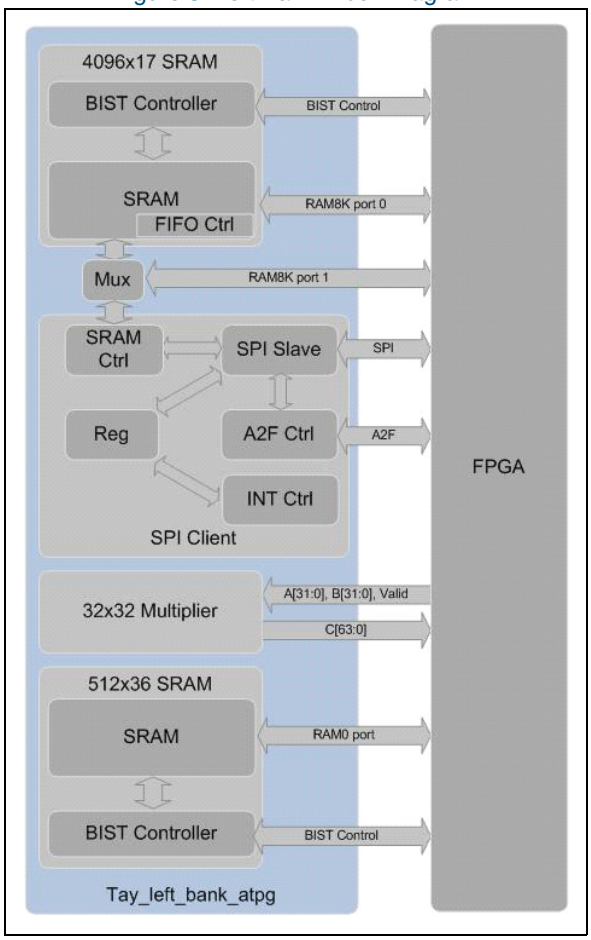
Table 5: Available Dual-Port Configurations

Number of RAM Blocks	Depth	Supported Widths
1	512	1-18 bits
2	512	1-36 bits
2	1024	1-18 bits
2	2048	1-9 bits

Left Bank

Figure 5 is functional block diagram of the left bank.

Figure 5: Left Bank Block Diagram



The left bank is composed of the following blocks:

- 32x32 multiplier
- Single-ported 512x36 SRAM (read/write)
- 8 KB (2048x32 SRAM) – write port 0 and read port 1 muxed with SPI slave interface
- SPI slave/client which includes SPI slave, A2F master, register block and SRAM interface to 8 KB SRAM

Figure 6 describes the left bank ports.

Table 6: Left Bank Ports

Port Name	Width	Direction	Description
System			
RESET_n	1	Input	System reset (active LOW).
SPI Interface			
SPI_CLK	1	Input	SPI clock. Main and only clock of the SPI slave block.
SPI_MOSI	1	Input	Serial input from SPI master.
SPI_SSn	1	Input	Slave select (active LOW).
SPI_MISO	1	Output	Serial out.
SPI_MISOe	1	Output	Serial out enable.
SPI Slave <-> FPGA			
A2F_GP_OUT	8	Output	General purpose out ASSP -> FPGA. This bus is driven by a register accessible through SPI.
A2F_GP_IN	8	Input	General purpose in FPGA -> ASSP. This bus is accessible using the SPI read command.
A2F_Control	8	Output	Control register output. [0] – A2F async I/F flush. [7:1] – TBD.
A2F_ADDR	8	Output	A2F Address bus. This bus is initialized through a SPI write and is self-incrementing.
A2F_WR_DATA	8	Output	A2F write data bus.
A2F_RD_DATA	8	Input	A2F read data bus.
A2F_REQ	1	Output	A2F request.
A2F_ACK	1	Input	A2F acknowledge.
A2F_RWn	1	Output	A2F Read (not Write) signal.
32x32 multiplier #0			
A_mult0	32	Input	Signed Operand A.
B_mult0	32	Input	Signed Operand B.
Valid_mult0	1	Input	Valid input.
C_mult0	64	Output	Signed output C.
ASSP_RAM 8K port 0			
RAM8K_P1_mux	1	Input	SRAM port 1 mux control. ‘0’ – 8 K RAM port 1 owned by SPI slave (default). ‘1’ – 8 K RAM port 1 owned by FPGA in use case where SPI slave is not used.
RAM8K_P0_CLK	1	Input	SRAM clock input.
RAM8K_P0_ADDR	11	Input	SRAM address.
RAM8K_P0_WR_DATA	32	Input	Write data.
RAM8K_P0_WR_EN	1	Input	Write enable (high asserted).
RAM8K_P0_WR_BE	4	Input	Write Byte enable.

Table 6: Left Bank Ports *(Continued)*

Port Name	Width	Direction	Description
ASSP RAM 8K port 1			
RAM8K_P1_CLK	1	Input	SRAM clock input.
RAM8K_P1_ADDR	11	Input	SRAM address.
RAM8K_P1_RD_DATA	32	Output	Read data.
RAM8K_P1_RD_EN	1	Input	Read enable.
ASSP_RAM_0			
RAM0_CLK	1	Input	SRAM clock input.
RAM0_ADDR	9	Input	SRAM address.
RAM0_WR_DATA	36	Input	Write data.
RAM0_RD_DATA	36	Output	Read data.
RAM0_WR_EN	1	Input	Write enable (high asserted).
RAM0_RD_EN	1	Input	Read enable (high asserted).
RAM0_WR_BE	4	Input	Write Byte enable.
Defaults			
af_opt_0	1	Input	SPI 8KB+2KB enable. '0' – SPI slave to RAM8K (default). '1' – SPI slave access to RAM8K and RAM0.
af_opt_1	1	Input	FPGA 8 KB RAM read enable. '0' – FPGA have write only access to RAM8K (default). '1' – FPGA have write and read access to RAM8K. Read access borrows RAM8K_P1_RD_DATA and RAM8K_P1_RD_EN ports.
af_dev_id	32	Input	Device ID.
af_spi_cpha	1	Input	SPI CPHA (tied to '0').
af_spi_cpol	1	Input	SPI CPOL (tied to '0').
af_spi_lsbf	1	Input	SPI LSBfirst (tied '0').
af_plat_id	8	Input	Platform ID (tied to 8'd26).

In addition to the ASSP ports, the left bank interface also has the oscillator ports to connect to the built-in oscillator. **Figure 7** describes the left bank oscillator ports.

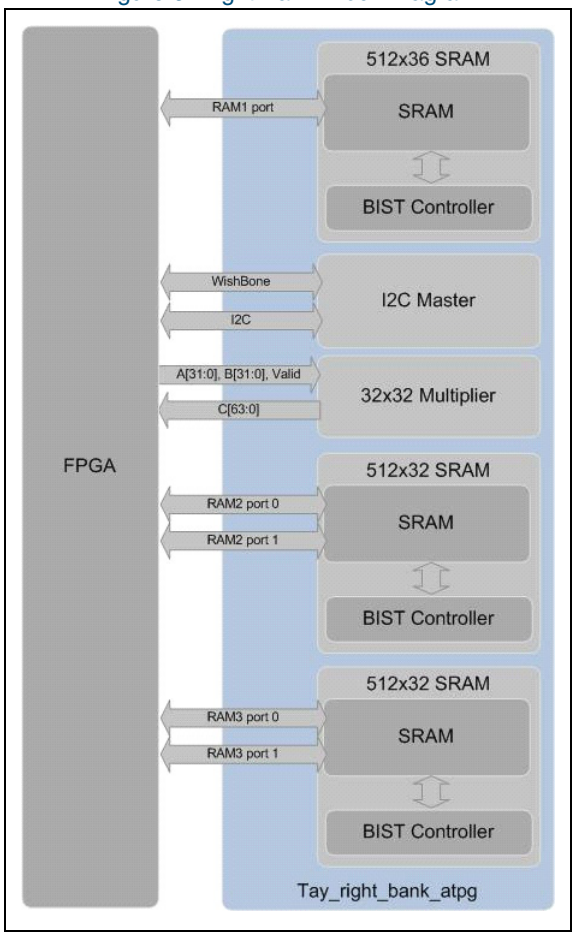
Table 7: Left Bank Oscillator Ports

Port Name	Width	Direction	Description
Oscillator			
osc_out	1	Output	Oscillator output to the FPGA
osc_en	1	Input	Oscillator Enable from FPGA (routable)
af_fast_osc_en	1	Input	Fast oscillator enable (tie-off)
af_256K_osc_en	1	Input	~256 kHz oscillator enable (tie-off)
af_128K_osc_en	1	Input	~128 kHz oscillator enable (tie-off)
af_64K_osc_en	1	Input	~64 kHz oscillator enable (tie-off)
af_32K_osc_en	1	Input	~32 kHz oscillator enable (tie-off)

Right Bank

Figure 6 is functional block diagram of the right bank.

Figure 6: Right Bank Block Diagram



The right bank is composed of the following blocks:

- 32x32 multiplier
- Single ported 512x36 SRAM (read/write)
- Two instances of dual-ported 512x32 SRAM (write port 0 and read port 1)
- I^2C master with internal wishbone bus interface

Table 8 describes the right bank ports.

Table 8: Right Bank Ports

Port Name	Width	Direction	Description
I²C Interface			
SCL_i	1	Input	SCL input.
SCL_o	1	Output	SCL output.
SCL_oen	1	Output	SCL output enable.
SDA_i	1	Input	SDA input.
SDA_o	1	Output	SDA output.
SDA_oen	1	Output	SDA output enable.
I²C master <-> FPGA			
wb_clk	1	Input	Clock input.
wb_rst	1	Input	Sync active high reset.
arst	1	Input	Async reset.
wb_adr	3	Input	Lower address bits.
wb_dat_i	8	Input	Data input.
wb_we	1	Input	Write enable.
wb_stb	1	Input	Strobe/core select.
wb_cyc	1	Input	Valid bus cycle.
wb_ack	1	Output	Bus cycle ACK.
wb_inta	1	Output	Interrupt request signal.
wb_dat_o	8	Output	Data output.
tip_o	1	Output	Txfer in-progress.
DrivingI2CBusOut	1	Output	Master is driving the I²C bus.
ASSP_RAM_1			
RAM1_CLK	1	Input	SRAM clock input.
RAM1_ADDR	9	Input	SRAM address.
RAM1_WR_DATA	36	Input	Write data.
RAM1_RD_DATA	36	Output	Read data.
RAM1_WR_EN	1	Input	Write enable (high asserted).
RAM1_RD_EN	1	Input	Read enable (high asserted).
RAM1_WR_BE	4	Input	Write Byte enable.
ASSP_RAM_2 port 0			
RAM2_P0_CLK	1	Input	SRAM clock input.
RAM2_P0_ADDR	9	Input	SRAM address.
RAM2_P0_WR_DATA	32	Input	Write data.
RAM2_P0_WR_EN	1	Input	Write enable (high asserted).
RAM2_P0_WR_BE	4	Input	Write Byte enable.

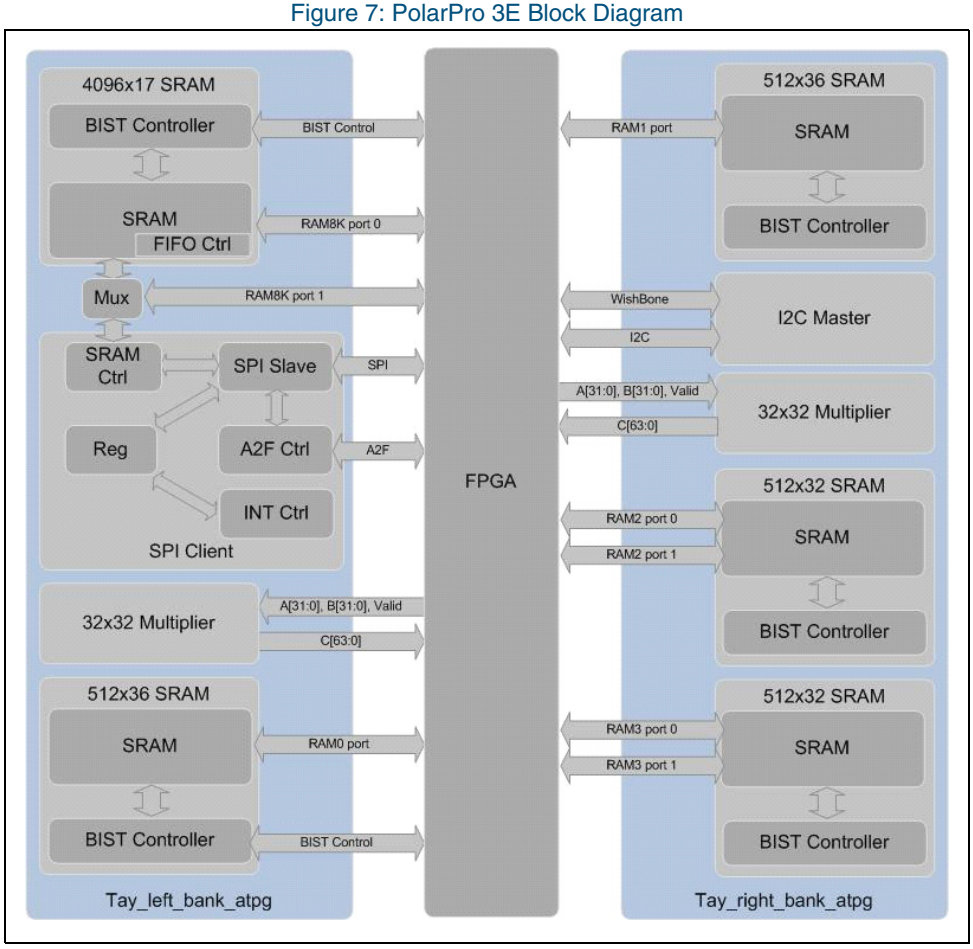
Table 8: Right Bank Ports *(Continued)*

Port Name	Width	Direction	Description
ASSP_RAM_2 port 1			
RAM2_P1_CLK	1	Input	SRAM clock input.
RAM2_P1_ADDR	9	Input	SRAM address.
RAM2_P1_RD_DATA	32	Output	Read data.
RAM2_P1_RD_EN	1	Input	Read enable (high asserted).
ASSP_RAM_3 port 0			
RAM3_P0_CLK	1	Input	SRAM clock input.
RAM3_P0_ADDR	9	Input	SRAM address.
RAM3_P0_WR_DATA	32	Input	Write data.
RAM3_P0_WR_EN	1	Input	Write enable (high asserted).
RAM3_P0_WR_BE	4	Input	Write Byte enable.
ASSP_RAM_3 port 1			
RAM3_P1_CLK	1	Input	SRAM clock input.
RAM3_P1_ADDR	9	Input	SRAM address.
RAM3_P1_RD_DATA	32	Output	Read data.
RAM3_P1_RD_EN	1	Input	Read enable (high asserted).

Left and Right Banks

Figure 7 shows a block diagram of the PolarPro3E. As illustrated, the left and the right banks do not have any direct interconnects between them. Any interconnects between the banks can only be done through the programmable logic.

Figure 7: PolarPro 3E Block Diagram



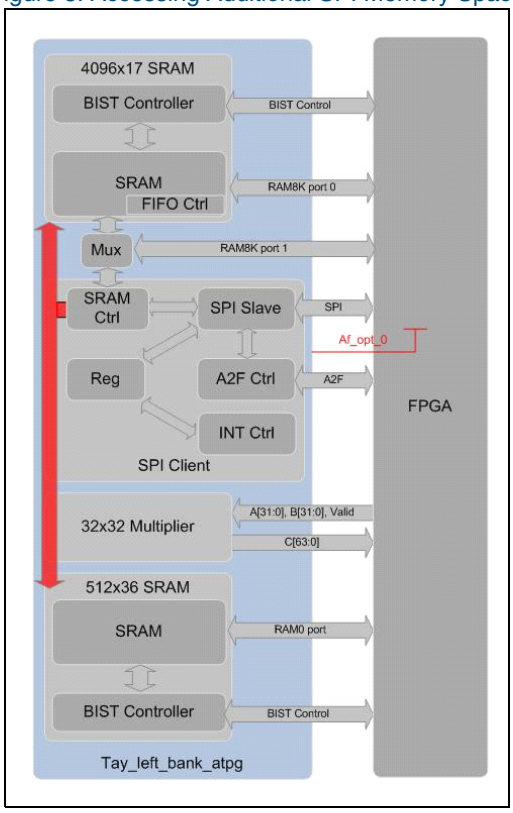
Additional Features

Some additional features are built into the PolarPro 3E that may be useful for some specific use case scenarios.

SPI Access to 8 KB + 2 KB SRAM

For some use cases, the 512x36 SRAM on the left bank can be left unused by the FPGA design. For these designs, there is an additional feature that allows extending the SPI memory space to include the 512x32 portion of this unused memory. A port named *af_opt_0*, when tied to '1' in the Verilog instantiation of the left bank, enables this path. **Figure 8** illustrates this path.

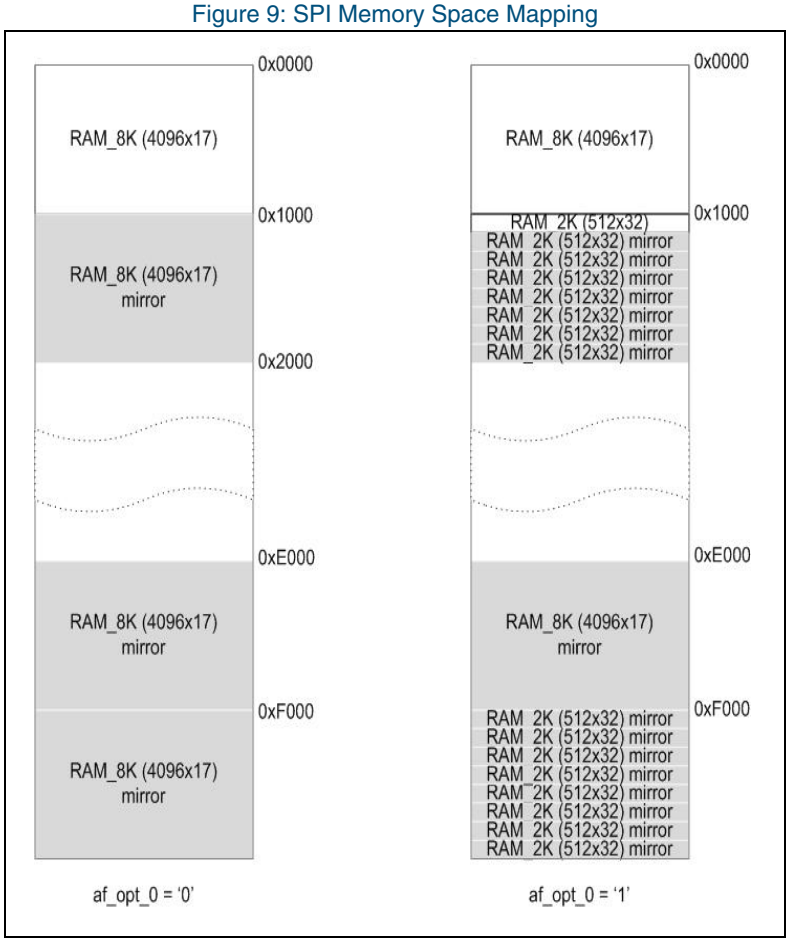
Figure 8: Accessing Additional SPI Memory Space



The SPI slave will have access to the 2048x32 and 512x36 RAMs (only 512x32 RAMs will be used). The FPGA side still has access these two SRAM through separate ports as usual.

One implication of this, aside from increasing the SPI accessible memory space from 8 KB (2048x32) to 10 KB (2560x32), is how the rest of the SPI addressable memory space is mapped and mirrored. The SPI command protocol allows for 16-bit addressing, which provides for 64 K locations. With *af_opt_0* at its default value, SPI memory space will be 2 K mirrored across the whole 64 K locations at 2 K boundaries. With *af_opt_0* =1, the actual SPI memory space becomes 2.5 K, mirrored across the 64 KB at 4 K boundaries. **Figure 9** illustrates this mapping.

Figure 9: SPI Memory Space Mapping

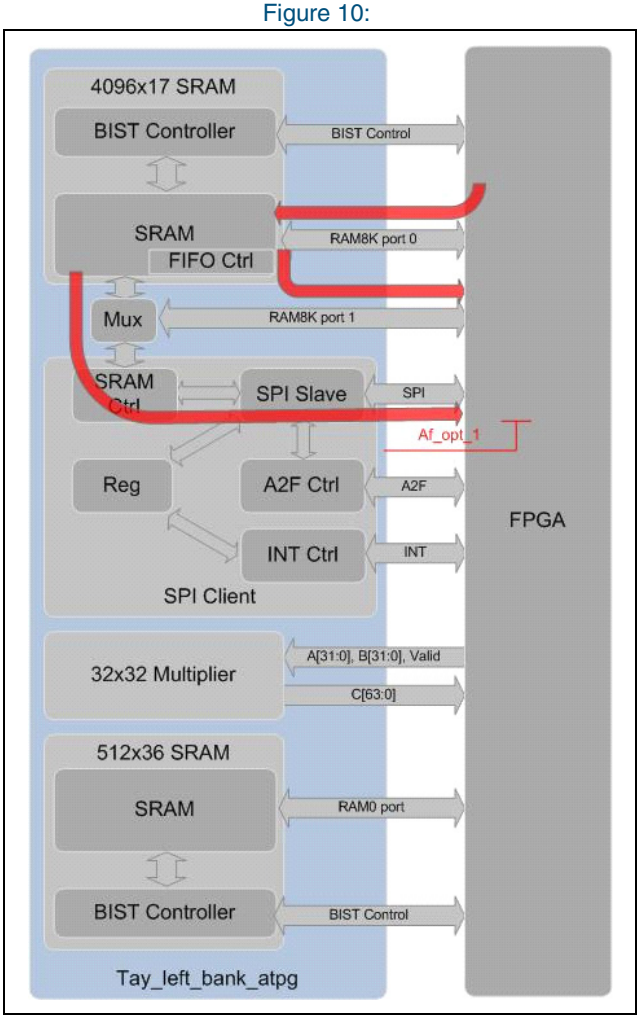


RAM8K FPGA Read Enable

In most use cases the SPI slave reads from the 8 KB SRAM data written by the FPGA design. The FPGA design uses the RAM8K write port0 to write to the RAM8K (using the reference clock *RAM8K_P0_CLK)*. The SPI slave reads from the RAM running at the *SPI_CLK* domain. The RAM8K read port1 is not used in this instance.

If *af_opt_1* is set to a '1', part of the RAM8K read port is used to allow the FPGA design to read the RAM8K. The two ports that are borrowed from RAM8K port 1 are *RAM8K_P1_RD_DATA* and *RAM8K_P1_RD_EN*. The resulting RAM8K FPGA port is still a single port (using the RAM port 0 *CLK* and address), but is a read/write port instead of a write only port. **Figure 10** illustrates this data path.

Figure 10:



True Dual-Port RAM

PolarPro 3E Dual-Port RAM modules can also be concatenated to generate True Dual-Port RAMs. The True Dual-Port RAM module's Port1 and Port2 have completely independent read and write ports and separate read and write clocks. This allows Port1 and Port2 to have different data widths and clock domains from each other. It is important to note that there is no circuitry preventing a write and read operation to the same address space at the same time. Therefore, the designer must ensure that the same address is not read from and written to simultaneously, otherwise the data is considered invalid. Likewise, the same address should not be written to from both ports at the same time. However, it is possible to read from the same address.

Figure 11 shows an example of a 1024x18 true dual-port RAM.

Figure 11: 1024x18 True Dual-Port RAM Block

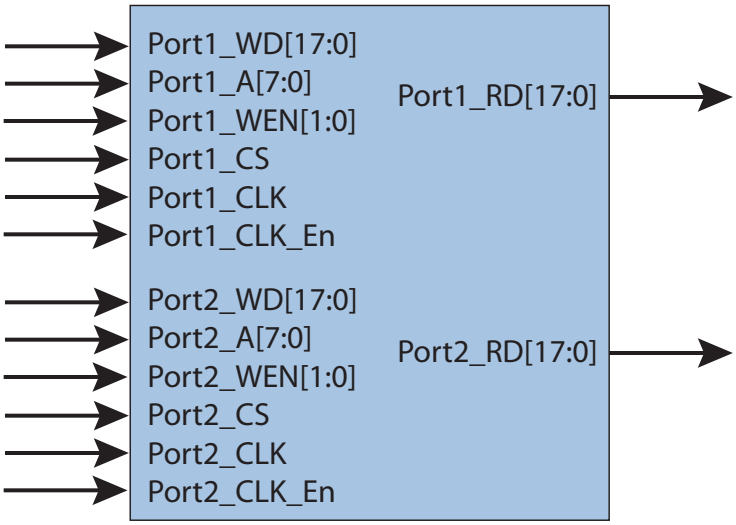


Table 9 describes the true dual-port RAM interface signals.

Table 9: True Dual-Port RAM Interface Signals

Port	Signal Name	Function
Port1	**Inputs**	
	Port1_WD [17:0]	Write Data
	Port1_A [9:0]	Write Address
	Port1_WEN	Write Enable
	Port1_CS	Chip Select
	Port1_CLK	Clock
	Output	
	Port1_RD [17:0]	Read Data
Port2	**Inputs**	
	Port2_WD [17:0]	Write Data
	Port2_A [9:0]	Write Address
	Port2_WEN	Write Enable
	Port2_CS	Chip Select
	Port2_CLK	Clock
	Output	
	Port2_RD [17:0]	Read Data

Table 10 lists the true dual-port configurations that are available.

Table 10: Available True Dual-Port Configurations

Number of RAM Blocks	Depth	Width
2	1024	1-18
2	2048	1-9

Embedded FIFO Controllers

Every 8-kilobit RAM block can be implemented as a synchronous or asynchronous FIFO. There are built-in FIFO controllers that allow for varying depths and widths without requiring programmable fabric resources. During asynchronous operation, the FIFO works in a half-duplex fashion such that PUSH is on one clock domain and POP is on another clock domain. The DIR signal allows the FIFO PUSH and POP signal directions to reverse. Refer to **Table 11** for details on the signal directions. It is important that FIFO pointers are flushed after DIR is switched to reset the FIFO pointers.

The PolarPro 3E FIFO controller features include:

- x9, x18 and x36 data bus widths
- Independent PUSH and POP clocks
- Independent programmable data width on PUSH and POP sides
- Configurable synchronous or asynchronous FIFO operation
- 4-bit PUSH and POP level indicators to provide FIFO status outputs for each port
- Pipelined read data to improve timing
- Option for inverted or non-inverted Async_Flush input

Table 11: FIFO Interface Signals

Signal Name	Width (bits)	Direction	Function
PUSH Signals			
DIN	1 to 36	I	Data bus input.
PUSH	1	I	Initiates a data push.
Fifo_Push_Flush	1	I	Empties the FIFO.
Push_Clk	1	I	Push data clock.
POP Signals			
DOUT	1 to 36	O	Data bus output.
POP	1	I	Initiates a data pop.
Fifo_Pop_Flush	1	I	Empties the FIFO.
Pop_Clk	1	I	Pop data clock.
Status Flags			
Almost_Full	1	O	Asserted when FIFO has one location available.
Almost_Empty	1	O	Asserted when FIFO has one location used.
PUSH_FLAG	4	O	FIFO PUSH level indicator.
POP_FLAG	4	O	FIFO POP level indicator.
Asynchronous Signals			
DIR	1	I	Determines the direction of the PUSH and POP signals: 0 – Signals set as normal. 1 – Reverses the FIFO direction so that the PUSH signals become POP signals and POP signals become PUSH signals.
Async_Flush	1	I	Asynchronous input to flush FIFO. Used to reset FIFO logic asynchronously.

Figure 12 shows an example a FIFO module.

Figure 12: PolarPro 3E FIFO Module

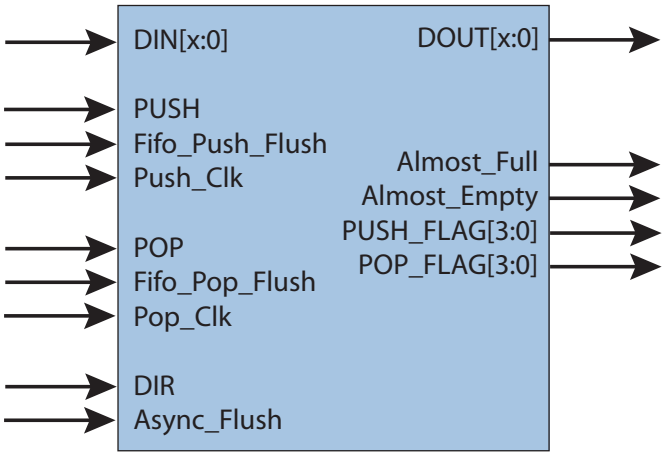


Table 12 lists the FIFO configurations that are available.

Table 12: Available FIFO Configurations

Number of RAM Blocks	Depth	Supported Widths
1	512	1-18 bits
2	512	1-36 bits
2	1024	1-18 bits
2	2048	1-9 bits

Table 13 and **Table 14** highlight the corresponding FIFO level indicator for each 4-bit value of the PUSH_FLAG and POP_FLAG outputs.

Table 13: FIFO PUSH Level Indicator Values

Value	Status
0000	Full
0001	Empty
0010	Room for more than one-half
0011	Room for more than one-forth
0100	Room for less than one-forth full to 64
1010	Room for 32 to 63
1011	Room for 16 to 31
1100	Room for 8 to 15
1101	Room for 4 to 7
1110	Room for at least 2
1111	Room for at least 1
Others	Reserved

Table 14: FIFO POP Level Indicator Signals

Value	Status
0000	Empty
0001	1 entry in FIFO
0010	At least 2 entries in FIFO
0011	At least 4 entries in FIFO
0100	At least 8 entries in FIFO
0101	At least 16 entries in FIFO
0110	At least 32 entries in FIFO
1000	Less than one-forth to 64 full
1101	One-forth or more full
1110	One-half or more full
1111	Full
Others	Reserved

FIFO Synchronous Flush Procedure

Both PUSH and POP domains are provided with a flush input signal synchronized to their respective clocks. When a flush is triggered from one side of the FIFO, the signal propagates and re-synchronizes internally to the other clock domain. During a flush operation, the values of the FIFO flags are invalid for a specific number of cycles (see **Figure 13** and **Figure 14**).

As shown in **Figure 13**, when the **Fifo_Push_Flush** asserts, the **Almost_Full** and **PUSH_FLAG** signals become invalid until the FIFO can flush the data with regards to the Push clock domain as well as the Pop clock domain. After the **Fifo_Push_Flush** is asserted, the next rising edge of the Pop clock starts the Pop flush routine.

Figure 13 illustrates a FIFO Flush operation. After the **Fifo_Push_Flush** is asserted at 2 (**PUSH_Clk**), two POP clock cycles (**11** and **12**) are required to update the **POP_FLAG**, and **PUSH_FLAG** signals. The **Almost_Empty** signal is asserted to indicate that the push flush operation has been completed. On the following rising edge of the **PUSH_Clk** (7), the **PUSH_FLAG** is accordingly updated to reflect the successful flush operation.

Figure 13: FIFO Flush from PUSH Side

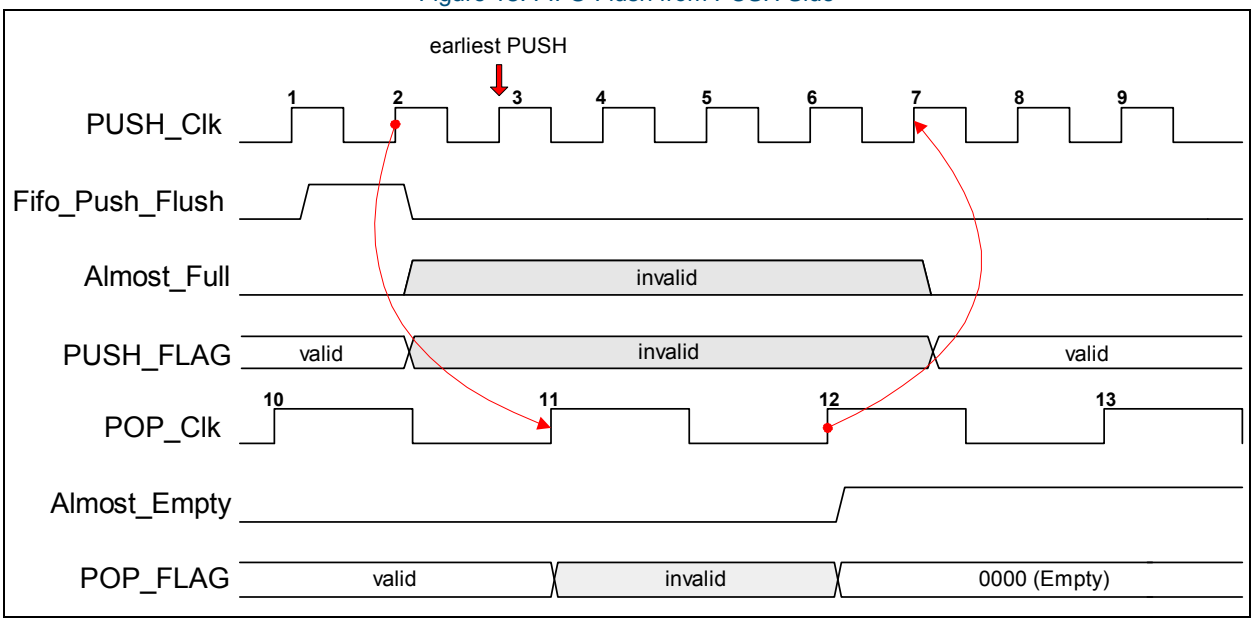


Figure 14 illustrates a POP flush operation. After the **Fifo_Pop_Flush** is asserted at 2 (**POP_Clk**), two PUSH clock cycles (**11** and **12**) are required to update the **POP_FLAG** and **PUSH_FLAG** signals. The **Almost_Empty** signal is asserted to indicate that the pop flush operation has been completed. On the following rising edge of the **POP_Clk** (7), the **POP_FLAG** is updated accordingly to reflect the successful flush operation.

Figure 14: FIFO Flush from POP Side

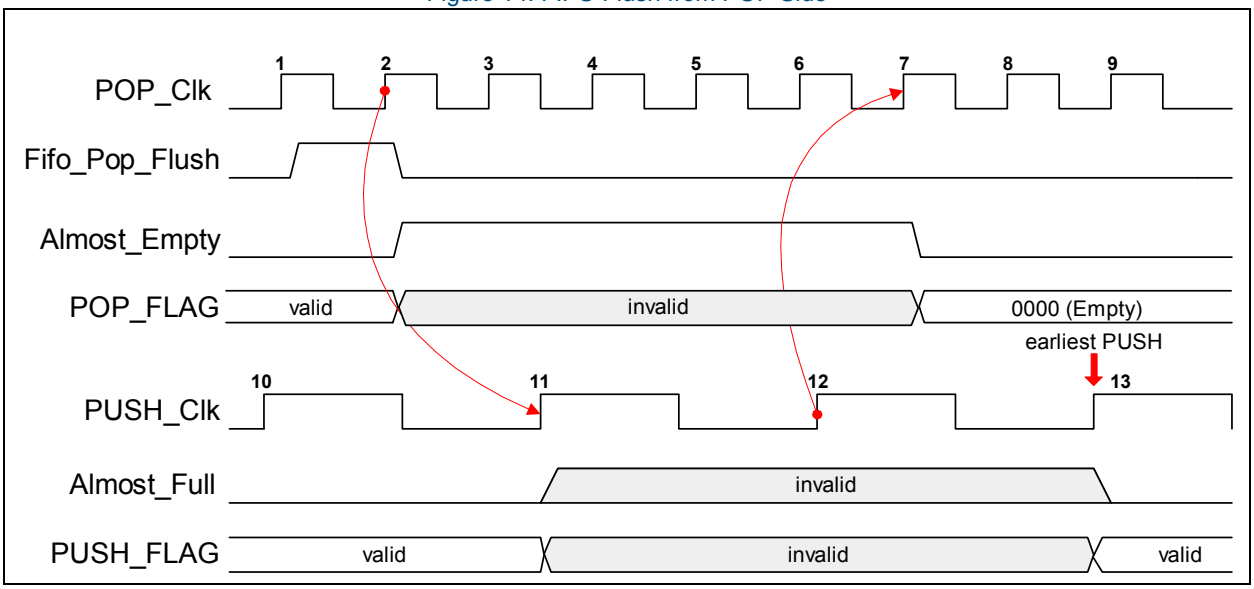


Figure 13 and **Figure 14** are only true for this particular PUSH-POP clock frequency combination. The clock frequency and phase difference between POP_Clk and PUSH_Clk can cause an additional flush delay of one clock cycle in either domain because of the asynchronous relationship between the two clocks.

FIFO Asynchronous Flush

Aside from the synchronous flush controls, there is an asynchronous flush signal named ASYNC_FLUSH. This signal is tied directly to the PUSH and POP pointers without any deglitching circuitry. The designer can add deglitching circuitry if desired.

32x32 Multiplier

To conserve programmable logic cells, two 32x32 combinatorial multipliers have been designed in hard logic on the PolarPro 3E. These 32x32 bit multipliers have the following features:

- 2x 32-bit input
- 64-bit output (lower 16-bit can be dropped to save interface signals)
- Signed multiplier
- Purely combinatorial (no option for accumulation, pipelining, shifting or saturation)
- Latched input

A simple block diagram of the multiplier is shown in **Figure 15**.

Figure 15: 32x32 Multiplier Block Diagram

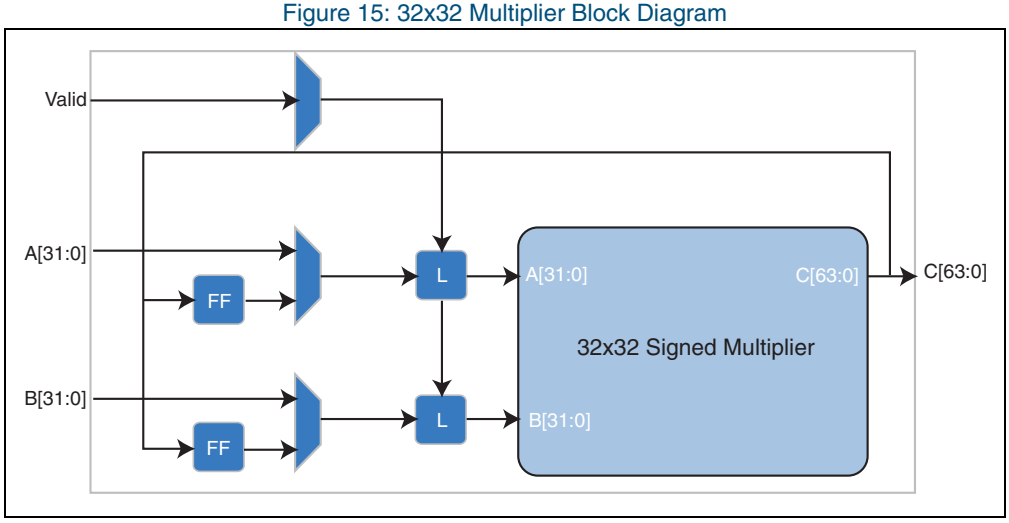


Table 15 shows the normal mode interface for the multiplier block.

Table 15: 32x32 Multiplier Normal Mode

Port Name	Width	Direction	Description
A	32	Input	Signed operand A (2's complement)
B	32	Input	Signed operand B (2's complement)
Valid	1	Input	Latch enable 1 = Latch pass-thru 0 = Latch off
C	64	Output	Signed product C (2's complement)

A pair of 32-bit latches are instantiated to latch in the two operands, controlled by an input latch enable signal called Valid.

- When Valid = '1' (HIGH), operands A and B are passed through into the internal combinatorial multiplier.
- When Valid = '0' (LOW), changes in A and B do not affect the multiplier.

Figure 16 shows the internal combinatorial multiplier.

Figure 16: Internal Combinatorial Multiplier

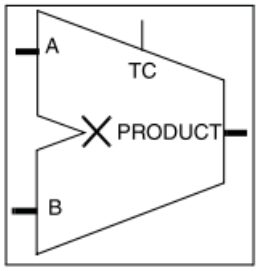


Table 16 defines the pins used on the internal combinatorial multiplier.

Table 16: Internal Combinatorial Multiplier Functional Description

Pin Name	Width	Direction	Function
A	A_*width* bit(s)	Input	Multiplier
B	B_*width* bit(s)	Input	Multiplicand
TC	1 bit	Input	Two's complement control 0 = unsigned 1 = signed
C	A_*width* + B_*width* bit(s)	Output	Product A x B

Distributed Clock Networks

Global Clocks

The PolarPro 3E clock network architecture consists of a 2-level H-tree network as shown in **Figure 17**. The first level of each clock tree (high-lighted in red) spans from the clock input pad to the global clock network and to the center of each quadrant of the chip. The second level spans from the quadrant clock network to the column clock network, and then to every logic cell inside that quadrant. There are five global clocks in the global clock network, and five quadrant clocks in each quadrant clock network. All global clocks drive the quadrant clock network inputs.

The quadrant clocks output to column clock buffers, which can be dynamically disabled at the column level. Column clock buffers can be implemented in Verilog, VHDL, and schematic designs by instantiating the column clock buffer macro, CAND. **Figure 18** shows the schematic representation of the CAND macro. The global clocks can drive RAM block clock inputs and reset, set, enable, and clock inputs to I/O registers. Furthermore, the quadrant clock outputs can be routed to all logic cell inputs.

Figure 17: PolarPro 3E Clock Architecture

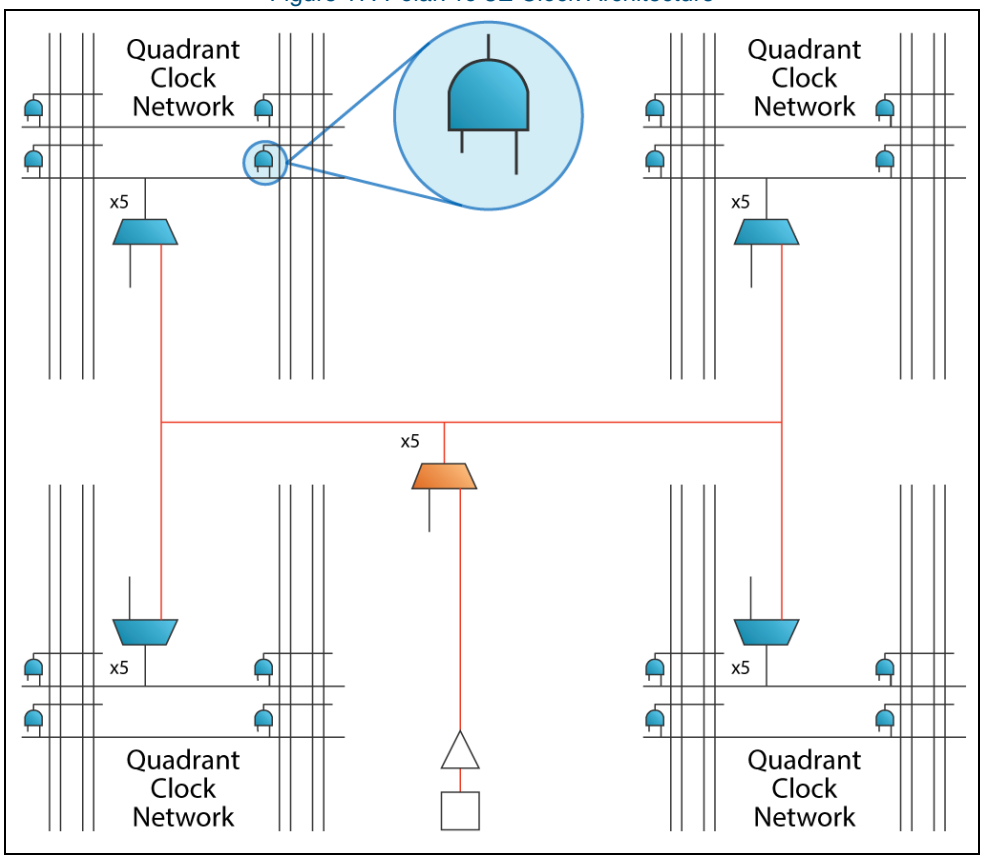
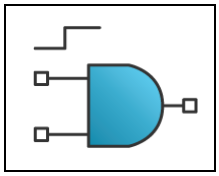


Figure 18: CAND Macro



The five global clock networks can either be driven directly by clock pads or internally generated signals. These global clocks go through 2-input global clock muxes located in the middle of the die. A diagram of a 2-input global clock mux is shown in **Figure 19**.

Figure 19: Global Clock Structure

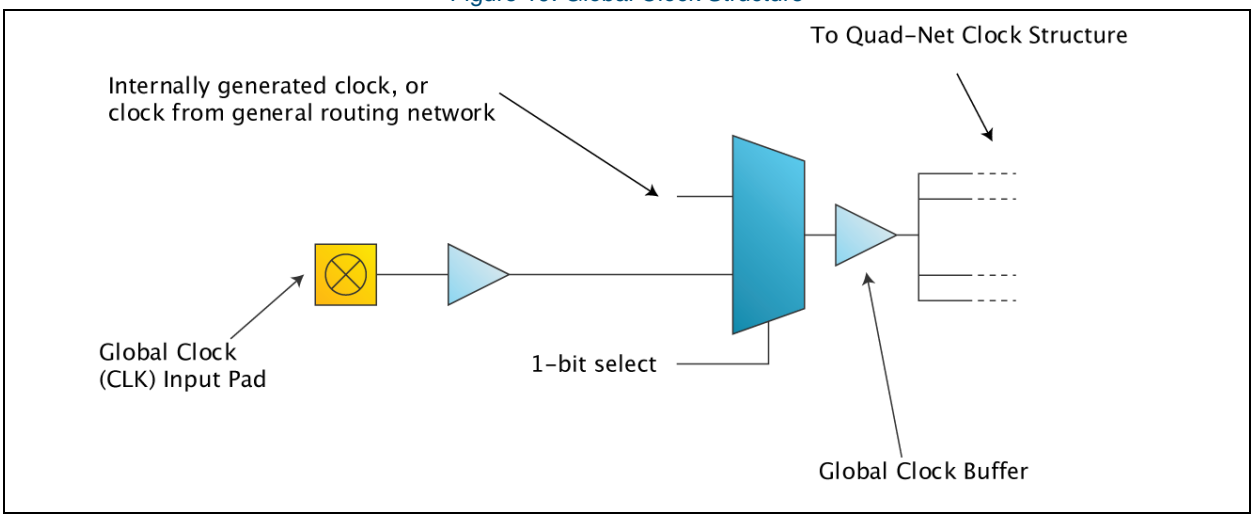
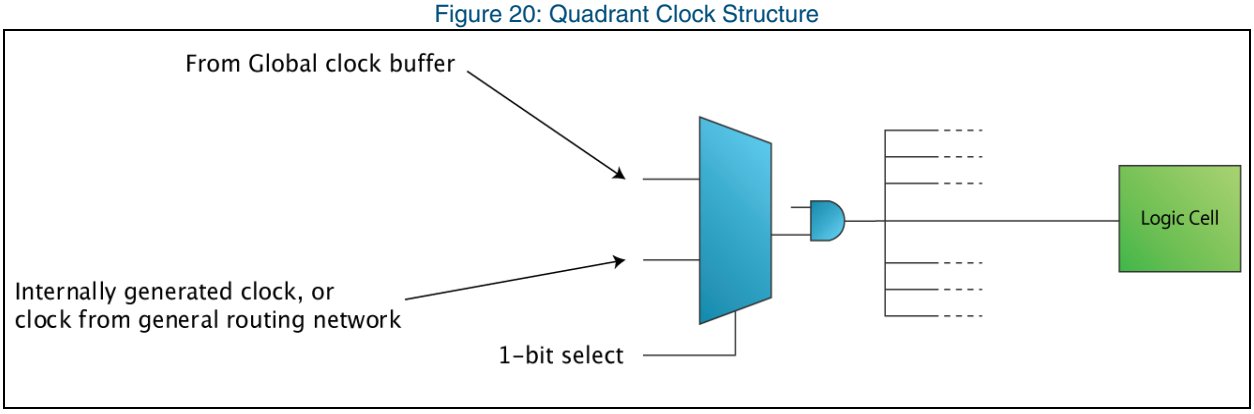


Figure 20 illustrates the quadrant clock 2-input mux.

Figure 20: Quadrant Clock Structure



NOTE: Select lines for the global clock and quadrant clock muxes are static signals and cannot be changed dynamically during device operation.

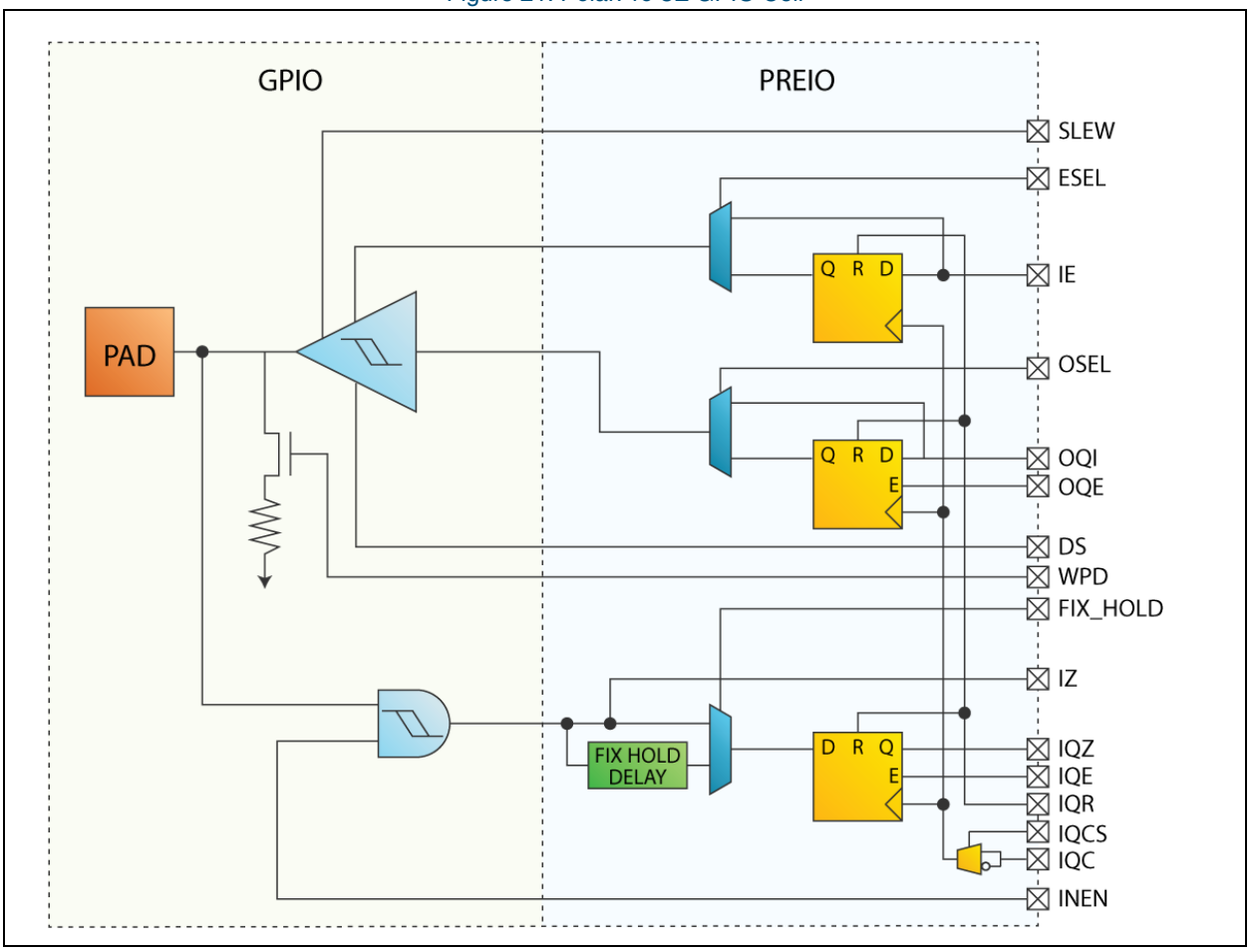
GPIO Cell Structure

The GPIO features include:

- Direct or registered input with input path select
- Direct or registered output with output path select
- Direct or registered output enable with OE path select
- Input buffer enable to reduce power
- Configurable pull-down control
- Inverted or non-inverted clock signal to flip-flops
- Two drive strength options

Figure 21 is a diagram of the PolarPro 3E GPIO cell.

Figure 21: PolarPro 3E GPIO Cell



With bi-directional I/O pins and global clock input pins, the PolarPro 3E device maximizes I/O performance, functionality, and flexibility. All input and I/O pins are 1.8 V, 2.5 V, and 3.3 V tolerant and comply with the specific I/O standard selected. For single ended I/O standards, the corresponding VCCIO bank input specifies the input tolerance and the output drive voltage.

Table 17 describes the GPIO interface signals.

Table 17: GPIO Interface Signals

Signal Name	Direction	Function
Routable Signals		
ESEL	I	Select signal for registered or non-registered output enable.
IE	I	Output enable signal.
OSEL	I	Select signal for registered or non-registered output signal.
OQI	I	Output signal.
OQE	I	Enable signal for output stage flip-flop.
IZ	O	Input data from pad.
IQZ	O	Registered input data from pad.
IQE	I	Enable signal for input stage flip-flop.
IQCS	I	Select signal for clock (inverted or non-inverted). This signal can only be tied high or low.
IQC	I	Clock signal to PREIO flip-flops.
IQR	I	Reset signal to all flip-flops within the GPIO cell.
INEN	I	Input enable signal.
Static Signals		
DS	I	Drive strength control.
WPD	I	Weak pull-down control signal.
FIX_HOLD	I	Additional delay module select signal.

Programmable Weak Pull-Down

A programmable weak pull-down controller is also available on each GPIO. The I/O pull-down eliminates the need for external resistors.

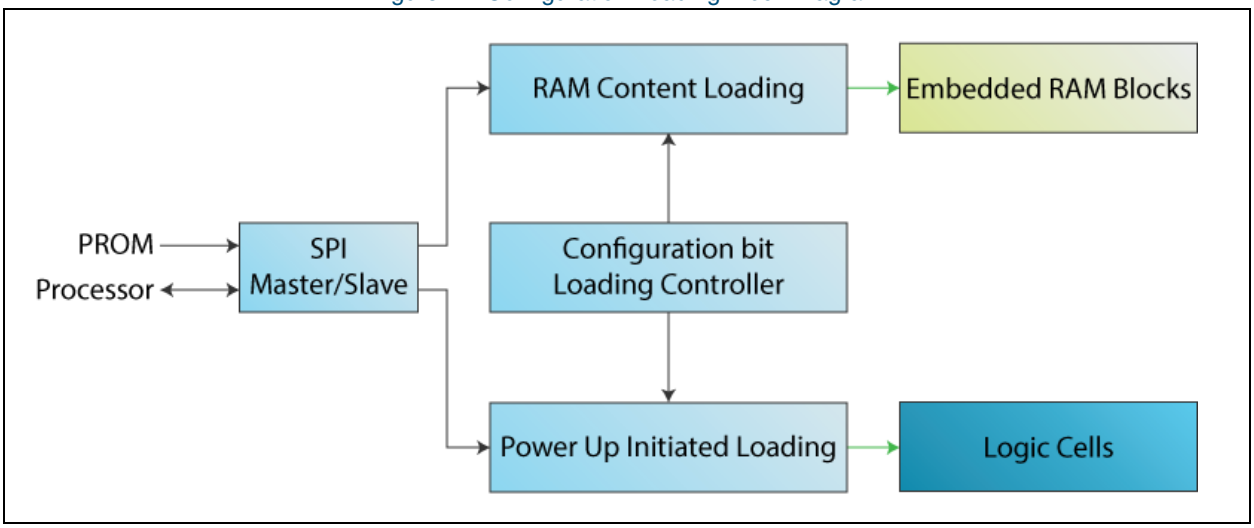
Programmable Weak Pull-Up

A programmable weak pull-up controller is available on selected GPIO (see the pinout table for details). The I/O pull-up can eliminate the need for external components.

PolarPro 3E Configuration Loading

The PolarPro 3E family of devices are reconfigurable. The configuration of a PolarPro 3E must be loaded each time the device is powered on. As shown in **Figure 22**, the PolarPro 3E provides two interfaces for configuring the logic cells and RAM blocks within the device. These two interfaces are SPI Master and SPI Slave.

Figure 22: Configuration Loading Block Diagram



SPI Modes of Operation

The configuration controller of the PolarPro 3E device can operate as a SPI Master or SPI Slave. When operating in SPI Master mode, PolarPro 3E devices read data from a Programmable Read-Only Memory (PROM). When operating in SPI Slave mode, PolarPro 3E receives data from a processor.

The SPI Slave interface is implemented in hard logic, and will consume significantly less power than a fabric-implemented SPI Master interface.

Operation in SPI Master mode or SPI Slave mode is determined by detecting either a logical high or low voltage on the SPI_CS_N pin upon de-assertion of SPI_RST_N.

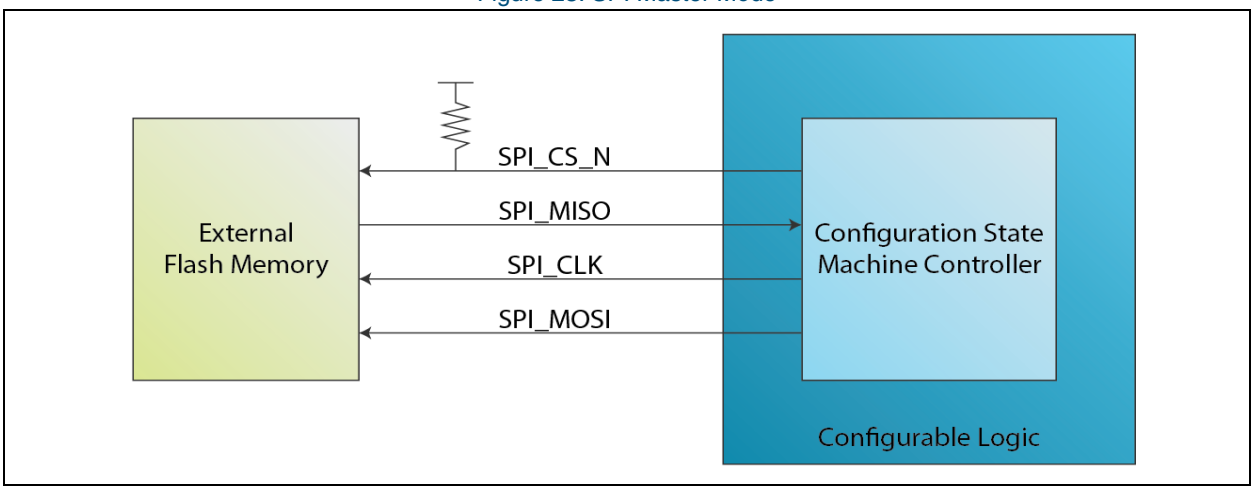
- When SPI_CS_N is high, the PolarPro 3E SPI controller enters SPI Master mode.
- When SPI_CS_N is low, the PolarPro 3E SPI controller enters SPI Slave mode.

Once configuration is completed, the SPI_CS_N, SPI_MOSI, SPI_MISO, and SPI_CLK signals will become normal GPIO.

SPI Master Mode

In SPI Master mode (shown in **Figure 23**), SPI_RST_N must be asserted to hold the PolarPro 3E in a reset state until the PROM is fully powered up and ready to be read. Upon de-assertion of SPI_RST_N, the PolarPro 3E is set to SPI Master mode and will then take control of the SPI pins, and start initiating the required SPI commands.

Figure 23: SPI Master Mode



Configuration loading of the PolarPro 3E requires a PROM of adequate size (at lease 1 Mbit). The PolarPro 3E SPI Master SPI clock frequency can operate at 4 MHz or 16 MHz during configuration. Once configuration is complete, the dual purpose SPI I/O pins can be used as normal GPIO. It is important to note that the VCCIO of the SPI pins for programming and normal operation must match the VCCIO of the PROM.

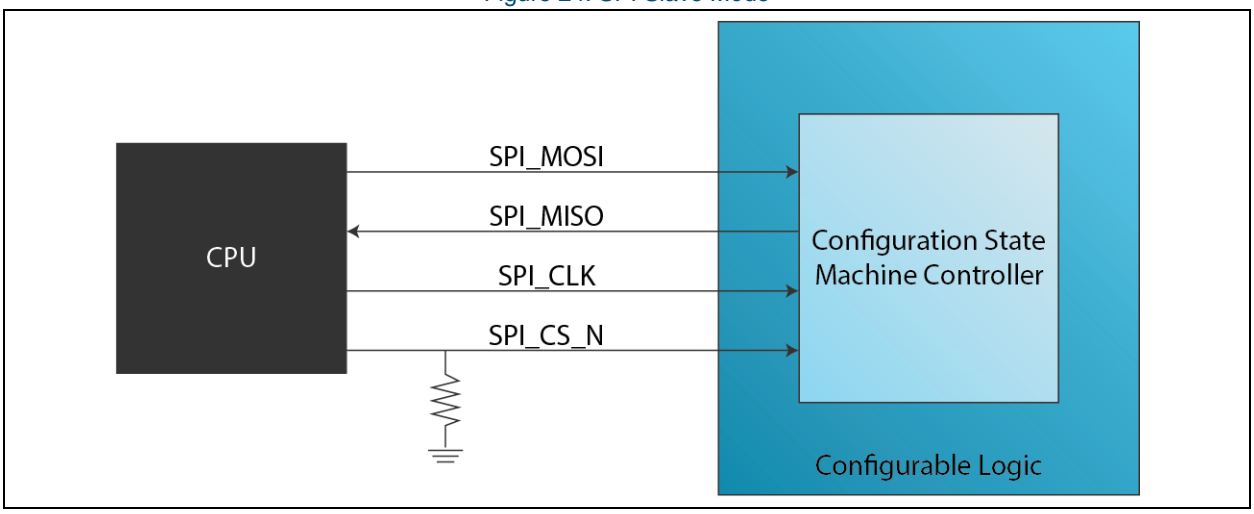
Upon completion of the loading, the PROM can be placed in a deep power down mode. To put the PROM into deep power down mode, the SPI Master sends a power down command after the last byte of data is received. Once the SPI pins switch to normal GPIO, and the PROM is in a deep power down mode, care must be taken to ensure that the PROM is not woken up unintentionally.

The PROM loading file used to program the external flash is generated by QuickLogic's QuickWorks software tools. The configuration data is constructed to work with the corresponding commands from the PolarPro 3E SPI Master.

SPI Slave Mode

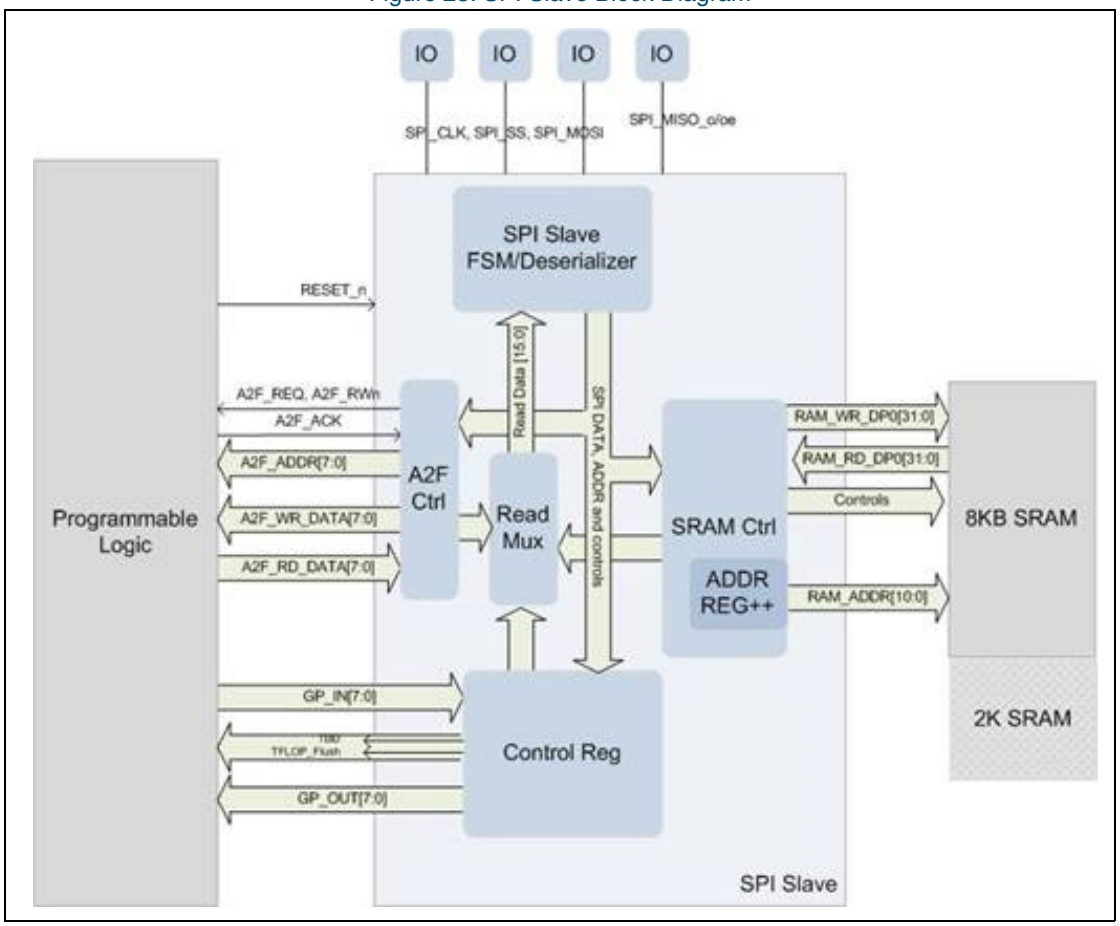
When the PolarPro 3E is powered up in SPI Slave mode (shown in **Figure 24**), the SPI Master takes control of the SPI pins. To initiate the data transfer, the SPI Master must assert the SPI_RST_N signal low for at least 20 ns to ensure the PolarPro 3 state machine is reset.

Figure 24: SPI Slave Mode



The configuration bit file, required for specifying the SPI Master commands, is generated by QuickLogic's QuickWorks software tools. The resulting binary file combined with software drivers supplied by QuickLogic can be used for configuration loading of the PolarPro 3E.

Figure 25: SPI Slave Block Diagram



The SPI slave is only active during normal operating mode, and is different from the SPI slave interface used for programmable logic configuration. These two SPI slaves are implemented separately and are not active at the same time. The normal mode SPI slave I/O can be programmed to use any of the GPIOs, while SPI I/O used by configuration SPI slave is predetermined and fixed. In normal systems where these two SPI slaves are used, the most likely scenario will have both using the same sets of I/Os.

Table 18 lists the ASSP -> FPGA (A2F) interface signals required by the SPI slave.

Table 18: SPI Slave Interface Signals

Port Name	Width	Direction	Description
System			
RESET_n	1	Input	System reset (active LOW).
SPI Interface			
SPI_CLK	1	Input	SPI clock. Main and only clock of the SPI slave block.
SPI_MOSI	1	Input	Serial input from SPI master.
SPI_SSn	1	Input	Slave select (active LOW).
SPI_MISO	1	Output	Serial out.
SPI_MISOe	1	Output	Serial out enable.
SPI Slave <-> FPGA			
A2F_GP_OUT	8	Output	General purpose out ASSP -> FPGA.This bus is driven by a register accessible through SPI.
A2F_GP_IN	8	Input	General purpose in FPGA -> ASSP. This bus is accessible using the SPI read command.
A2F_Control	8	Output	Control register output: [0] - A2F enable [1] - SPI ram access enable [7:2] - unused
A2F_Status	7	Input	Status. [6:0] - mapped to SPI Status register [7:1].
A2F_ADDR	8	Output	A2F address bus. This bus is initialized through a SPI write and is self-incrementing.
A2F_WR_DATA	8	Output	A2F write data bus.
A2F_RD_DATA	8	Input	A2F read data bus.
A2F_REQ	1	Output	A2F request.
A2F_ACK	1	Input	A2F acknowledge.
A2F_RWn	1	Output	A2F Read (not Write) signal.

SPI Protocol

The SPI bus transfers will support SPI mode 0 protocol. A full SPI access is delimited by the SPI_CSb transition. The first byte after the SPI_CSb assertion is decoded as the SPI command. SPI command has the following format:

Bit [7]: R/#W
0= write access
1= read access
Bit [6]: 16/ 8 bit address select
0 = 8 bit address
1= 16 bit address
Bit [5]: Burst Access
0= Single access
1= burst access
Bit [4]: Dummy byte for Burst read
0 = No dummy byte between read data during burst mode
1 = 1 dummy byte between each read data byte during burst mode
Bit [3:2]: Chip Select
00 = CS0, Register Access (8-bit data and 8-bit addr, burst not supported)
01 = CS1, 8KB SRAM access (32-bit data and 16-bit addr)
10 = CS2, A2F Access (8-bit data and 8-bit addr)
11 = CS3, Reserved
Bit [1:0]: data width select
00 = 8 bit data width
01 = Reserved
10 = 32-bit data width
11 = Reserved

SPI accesses to the PolarPro 3E have three possible targets: SPI slave local register, 8 KB SRAM and the internal A2F bus. The targets are detailed in **Table 19**.

Table 19: SPI Accesses

CS	Target	Address Locations	Data Width
00	SPI Local Register	256	8
01	8KB SRAM	2048	32
10	A2F Bus	256	8
11	Reserved		

I²C Master

A hard logic I²C master is included to allow the PolarPro 3E to read external I²C slaves. The I²C master block has the following interfaces listed in **Table 20**.

Table 20: I²C Master Interface

Port Name	Width	Direction	Description
I²C Interface			
SCL_i	1	Input	SCL input
SCL_o	1	Output	SCL output
SCL_oen	1	Output	SCL output enable
SDA_i	1	Input	SDA input
SDA_o	1	Output	SDA output
SDA_oen	1	Output	SDA output enable
I²C Master <-> FPGA			
wb_clk	1	Input	Clock input
wb_rst	1	Input	Sync active high reset
arst	1	Input	Async reset
wb_adr	3	Input	Lower address bits
wb_dat_i	8	Input	Data input
wb_we	1	Input	Write enable
wb_stb	1	Input	Strobe/core select
wb_cyc	1	Input	Valid bus cycle
wb_ack	1	Output	Bus cycle ACK
wb_inta	1	Output	Interrupt request signal
wb_dat_o	8	Output	Data output
tip_o	1	Output	Txfer in-progress
DrivingI2CBusOut	1	Output	Master driving I2C bus

Internal Oscillator

The PolarPro 3E has a included ring oscillator to best achieve low power system design. The PolarPro 3E designs require a clock source, which in most systems is present in the form of a 32 kHz clock. However, a 32 kHz clock might not be fast enough for some designs requiring more complicated computation per sample. Instead of requiring the system to provide the PolarPro 3E with an external clock source, the PolarPro 3E includes an internal oscillator that can be used during normal operating mode.

Figure 26 shows a block diagram of the internal oscillator design.

Figure 26: Internal Oscillator Block Diagram

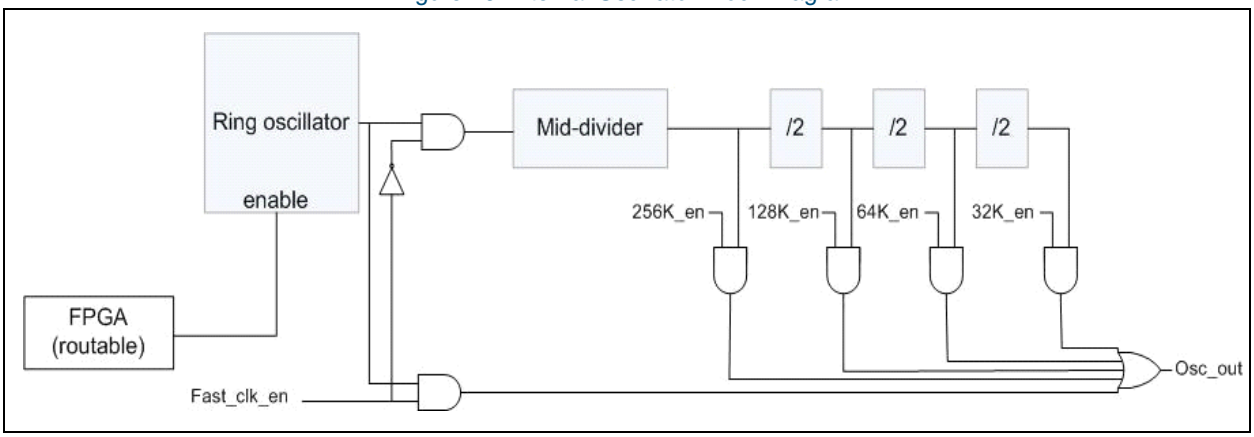


Table 21 lists and describes the internal oscillator interfaces.

Table 21: Internal Oscillator Interface

Port Name	Width	Direction	Description
Osc_out	1	Output	Oscillator output to the FPGA
Osc_en	1	Input	Oscillator Enable from FPGA (routable)
af_fast_osc_en	1	Input	Fast oscillator enable (tie-off)
af_256K_en	1	Input	~256 kHz oscillator enable (tie-off)
af_128K_en	1	Input	~128 kHz oscillator enable (tie-off)
af_64K_en	1	Input	~64 kHz oscillator enable (tie-off)
af_32K_en	1	Input	~32 kHz oscillator enable (tie-off)

The *OSC_en* signal comes from a software programmable register in the fabric. The divider selection bits (*fast_osc_en*, *256K_en*, *128K_en*, *64K_en* and *32K_en*) are tie-offs (defaults) and are mutually exclusive. Only one of these can be tied to a '1' for proper operation.

Configuration Verification Check Sum

To achieve higher system robustness, PolarPro 3E uses a checksum algorithm to guarantee data integrity. Upon receiving the data from the PROM, a check sum mechanism is used to ensure the PolarPro 3E configuration and embedded RAM data is intact. The final checksum is compared to those in the PROM checksum. If the checksums match, the CFG_DONE pin will go high. If the check sum does not match, the configuration controller retries configuration up to five times.

More details on programming PolarPro 3E devices are located in the *PolarPro 3E Configuration Loading User Guide*.

Electrical Specifications

DC Characteristics

The DC Specifications are provided in **Table 22** through **Table 31**.

Table 22: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
VCC Voltage	-0.5 V to 1.26 V	ESD Pad Protection	2 kV
VCCIO Voltage	-0.5 V to 3.6 V	Laminate Package (BGA) Storage Temperature	-55° C to + 125° C
Input Voltage	-0.5 V to 3.6 V	Latch-up Immunity	±100 mA

Table 23: Recommended Operating Range

Symbol	Parameter	Min.	Max.	Unit
VCC	Supply Voltage	1.14	1.26	V
VCCIO	Input Tolerance Voltage	1.71	3.6	V
TJ	Junction Temperature	-20	85.0	°C

Table 24: DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_I	I or I/O Input Leakage Current	VI = VCCIO or GND	-	1		µA
I_{OZ}	3-State Output Leakage Current	VI = VCCIO or GND	-	1		µA
C_I	I/O Input Capacitance	VCCIO = 3.6 V	-	5		pF
C_{CLOCK}	Clock Input Capacitance	VCCIO = 3.6 V	-	5		pF
I_{OS}	Output Short Circuit Current[a]	VO = GND		100		mA
		VO = VCC		60		mA
I_{PD}	Current on Programmable Pull-Down	VCCIO = 1.8 V	-	94		µA
		VCCIO = 3.6 V	-	90	160	µA
I_{PU}	Current on Programmable Pull-Up	VCCIO = 1.8 V		104		µA
I_{VCCIO}	Quiescent Current on VCCIO	VCCIO = 3.6 V	-	4		µA
		VCCIO = 2.5 V	-	4		µA
		VCCIO = 1.8 V	-	3.5		µA

a. This data represents the JEDEC and PCI specifications.

Table 25: DC Input and Output Levels[a]

Symbol	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MAX}	V_{MIN}	mA	mA
LVTTL	-0.3	0.8	2.2	VCCIO + 0.3	0.4	2.4	2.0	-2.0
LVCMOS25	-0.3	0.7	1.7	VCCIO + 0.3	0.4	1.8	2.0	-2.0
LVCMOS18	-0.3	0.63	1.17	VCCIO + 0.3	0.45	VCCIO - 0.45	2.0	-2.0

a. The data in this table represents JEDEC specifications. QuickLogic devices either meet or exceed these requirements. Based on weak pull-down I/O termination disabled.

Table 26: Quiescent Current

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{VCC}	Quiescent Current on VCC[a]	-	145	-	µA
I_{VCCIO}	Quiescent Current on VCCIO banks A, B, C, and D combined	-	2	-	µA
I_{VCCIO_E}	Quiescent Current on CFG_DONE and SPI_RST_N pins	-	2	-	µA

a. Based on typical process, single cell usage, all outputs tri-stated, and all inputs held at VCCIO or GND.

Table 27: GPIO Programmable Drive Strength

Drive Strength[a]	IOH (mA)			IOL (mA)		
	1.8 V	2.5 V	3.3 V	1.8 V	2.5 V	3.3 V
0	14	30	41	14	17	20
1	16	35	51	20	21	24

a. Values are based on input and output levels in **Table 25**.

Table 28: Slew Rates — VCCIO = 3.3V

VCCIO= 3.3V		25C VCCIO=3.3V / VCC=1.20V				85C VCCIO=3.0V / VCC = 1.14V			
		DS=0		DS=1		DS=0		DS=1	
		Rise (ns)	Fall (ns)	Rise (ns)	Fall (ns)	Rise (ns)	Fall (ns)	Rise (ns)	Fall (ns)
Fast-Fast	AC# 100.55 ns	3.13	2.29	2.80	2.11	3.46	2.51	3.14	2.28
Typical-Typical	AC# 113.12 ns	3.15	2.31	2.83	2.13	3.44	2.50	3.12	2.27
Slow-Slow	AC# 113.12 ns	3.15	2.33	2.84	2.14	3.44	2.52	3.12	2.30

Table 29: Slew Rates — VCCIO = 2.5V

VCCIO=2.5V		25C VCCIO=2.50V / VCC=1.20V				85C VCCIO=2.25V / VCC = 1.14V			
		DS=0		DS=1		DS=0		DS=1	
		Rise (ns)	Fall (ns)	Rise (ns)	Fall (ns)	Rise (ns)	Fall (ns)	Rise (ns)	Fall (ns)
Fast-Fast	AC# 157.45 ns	3.63	2.63	3.24	2.37	4.31	3.03	3.72	2.70
Typical-Typical	AC# 172.53 ns	3.64	2.66	3.25	2.40	4.25	3.03	3.70	2.70
Slow-Slow	AC# 211.12 ns	3.61	2.66	3.24	2.40	4.25	3.04	3.69	2.71

Table 30: Slew Rates — VCCIO = 1.8V

VCCIO=1.8V		25C VCCIO=1.80V / VCC=1.20V				85C VCCIO=1.71V / VCC = 1.14V			
		DS=0		DS=1		DS=0		DS=1	
		Rise (ns)	Fall (ns)	Rise (ns)	Fall (ns)	Rise (ns)	Fall (ns)	Rise (ns)	Fall (ns)
Fast-Fast	AC# 157.45 ns	3.80	3.03	3.13	2.74	4.40	3.35	3.51	3.00
Typical-Typical	AC# 172.53 ns	3.79	3.04	3.14	2.76	4.39	3.35	3.51	3.01
Slow-Slow	AC# 211.12 ns	3.78	3.06	3.14	2.74	4.43	3.38	3.52	3.03

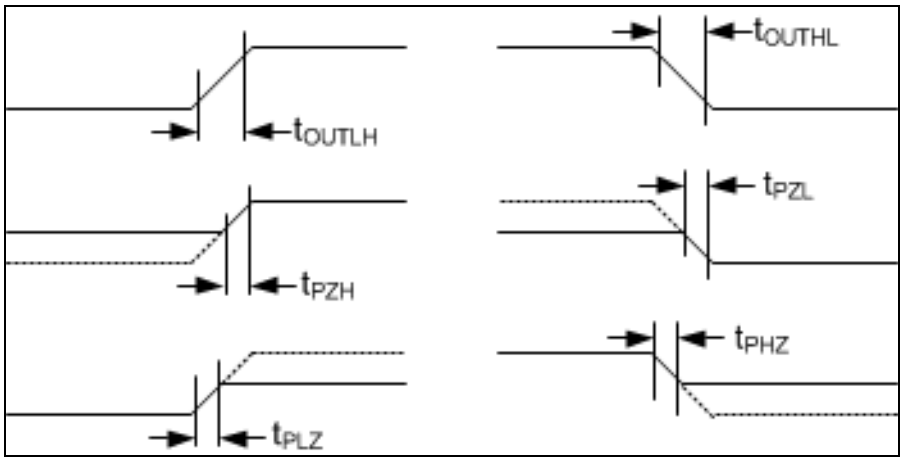
Table 31: Output Slew Rate

Symbol	Parameter[a]	VCCIO (V)	Drive Strength = 1 (ns)	Drive Strength = 0 (ns)
t_{PZH}	Output Delay tri-state to high (90% of H)	3.3	4.1	4.3
		2.5	4.6	4.8
		1.8	4.7	5.2
t_{PZL}	Output Delay tri-state to low (10% of L)	3.3	2.4	2.6
		2.5	2.7	2.9
		1.8	2.9	3
t_{PHZ}	Output Delay high to tri-state	3.3	25.2	27.9
		2.5	25.8	28.3
		1.8	26.7	27.6
t_{PLZ}	Output Delay low to tri-state	3.3	20.1	21.2
		2.5	20.4	22.0
		1.8	23.6	25.8

a. Based on 15pF load.

NOTE: t_{PHZ} and t_{PLZ} are measured at 0.5 VCCIO using a 0.5 K resistor on the open drain outputs.

Figure 27: Output Slew Rate



SPI Timing Characteristics

The SPI specifications are provided in **Table 32** through **Table 37**.

Table 32: SPI Master Timing

Symbol	Parameter	Value	
		Slow SPI_CLK	Fast SPI_CLK
t_{MFCMIN}	Minimum time from de-assertion of CFG_RST_N to the first SPI_CLK rising edge.	115 µs	115 µs
t_{MSUMIN}	Minimum setup time that the SPI Master output data will give before a SPI_CLK sampling edge.	105 ns	26 ns

When operating as the SPI Master, the PolarPro 3E initially reads an external SPI flash device using a slow clock (~4 MHz). After reading one byte, it determines whether it will switch over to use the fast clock (~16 MHz) or not. This improves configuration time by a factor of four for SPI flash devices that can support the speed.

Table 33: SPI Master SPI_CLK Timing

SPI Mode	Parameter	Value
SPI Master	Slow Output Frequency Range	4 MHz ±30%
	Fast Output Frequency Range	16 MHz ±30%

Table 34: SPI Slave Timing

Symbol	Parameter	Value	
		Slow SPI_CLK	Fast SPI_CLK
t_{SFCMIN}	Minimum time from de-assertion of CFG_RST_N to when the first SPI_CLK rising edge can be sent to the PolarPro 3E.	20 ns	20 ns
t_{SSUMIN}	Minimum setup time that the SPI_MOSI requires for input data.	9 ns	9 ns
t_{SHMIN}	Minimum hold time that the SPI_MOSI signal needs after sampling the data relative to the SPI_CLK edge.	300 ps	300 ps

Table 35: SPI Slave SPI_CLK Timing

SPI Mode	Parameter	Value
SPI Slave	SPI_CLK Input Frequency Range	200 kHz to 25 MHz

Table 36: SPI_RST_N Timing

Symbol	Parameter	Value
$t_{RST\_BGN\_MIN}$	Minimum time, after the VCC and VCCIO rails have reached their voltage, that SPI_RST_N should be high before asserting.	250 µs
$t_{RST\_ASRT\_MIN}$	Minimum time that SPI_RST_N must be asserted to reset the device correctly, and begin configuration.	20 ns

Table 37: CFG_DONE Timing

Symbol	Parameter	Value
t_{CFG_DONE}	Time from when CFG_DONE goes high, to when the device begins operation.	320 ns

Programmable Fabric

Table 38 shows the logic cell delays in the programmable fabric.

Table 38: Logic Cell Delays

Symbol	Parameter	Min.	Max.
t_{PD}	Combinatorial delay of the longest path: time taken by the combinatorial circuit to output	0.38 ns	0.79 ns
t_{SU}	Setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	0.19 ns	0.34 ns
t_{HL}	Hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0 ns	N/A
t_{ESU}	Enable setup time: time the enable input of the flip-flop must be stable before the active clock edge	0.68 ns	1.24 ns
t_{EHL}	Enable hold time: time the enable input of the flip-flop must be stable after the active clock edge	0 ns	0 ns
t_{CO}	Clock-to-out delay: the amount of time taken by the flip-flop to output after the active clock edge	0.25 ns	0.51 ns
t_{CWHI}	Clock high time: required minimum time the clock stays high	600 ps	600 ps
t_{CWLO}	Clock low time: required minimum time that the clock stays low	600 ps	600 ps
t_{SET}	Set delay: time between when the flip-flop is “set” (high) and the output is consequently “set” (high)	0.48 ns	0.88 ns
t_{RESET}	Reset delay: time between when the flip-flop is “reset” (low) and the output is consequently “reset” (low)	0.41 ns	0.69 ns
t_{SW}	Set width: time that the SET signal must remain high/low	300 ps	300 ps
t_{RW}	Reset width: time that the RESET signal must remain high/low	300 ps	300 ps

Figure 28 illustrates the logic cell flip-flop timings.

Figure 28: Logic Cell Flip-Flop Timings — First Waveform

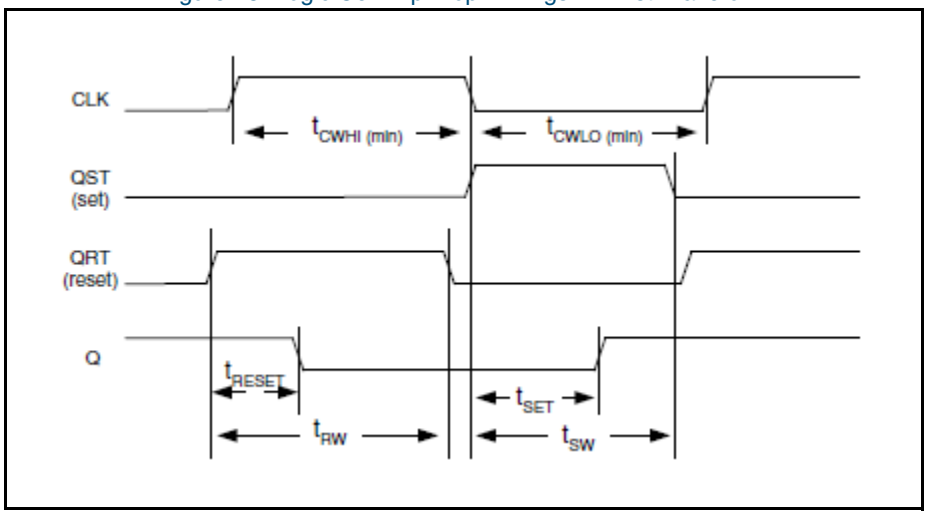


Table 39 shows the tree clock delays in the programmable fabric.

Table 39: Clock Tree Delay

Clock Segment	Parameter	Min.	Max.
t_{PGCK}	Clock pad to flip-flop	0.62 ns	1.42 ns
t_{PGMCK}	Global mux output to flip-flop	0.51 ns	1.17 ns
t_{PQDCK}	Quadrant mux output to flip-flop	0.35 ns	0.80 ns
t_{GSKEW}	Global delay clock skew	3.8 ps	8.3 ps

Power-Up Sequencing

Figure 29: Power-Up Sequencing

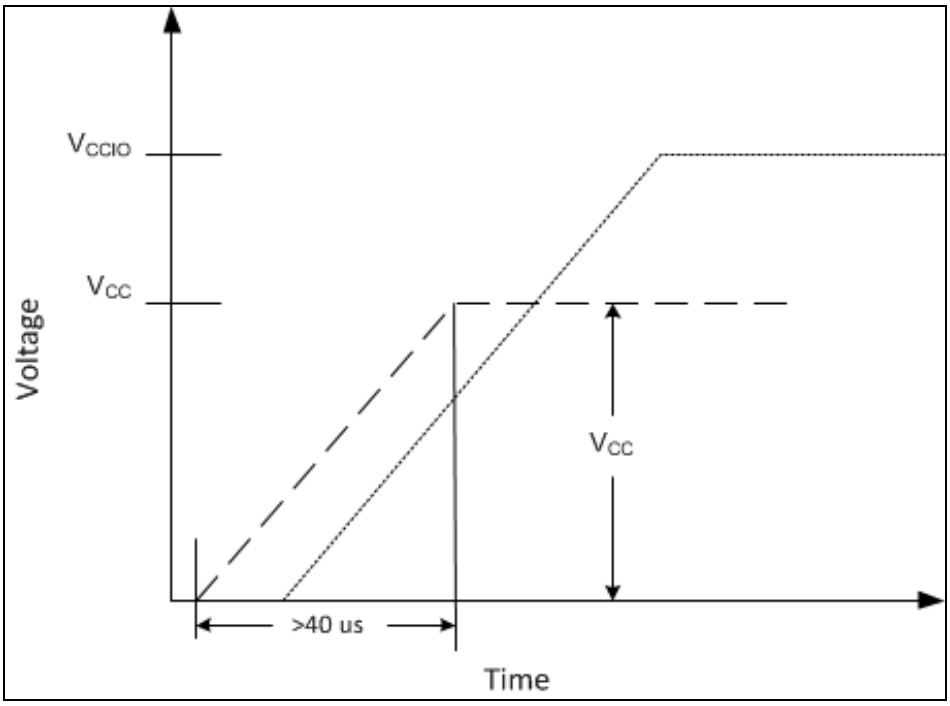


Figure 29 shows an example where all VCCIO = 3.3 V. When powering up a PolarPro 3E device, VCC and VCCIO rails must take 40 µs or longer to reach their maximum values. Ramping VCC and VCCIO faster than 40 µs can cause the device to behave improperly. It is also important to ensure VCC precedes VCCIO. In the case where VCCIO ramps up prior the VCC, additional current will be drawn. SPI_RST_N should not be asserted until 250 µs after VCC reaches its full voltage level.

Power Consumption

QuickLogic's low power reconfigurable logic is ideal for implementing connectivity solutions, custom logic and processor interfaces. The quiescent current can be as low as 145 µA. The dynamic power consumption varies depending on the operating conditions and what functions are used in the logic cells. Contact your QuickLogic Customer Solution Architect (CSA) for specifics related to your use case.

Moisture Sensitivity Level

Table 40 describes the solder composition characteristics.

Table 40: Solder and Lead Finish Composition

Package Type[a]	Ball Count	Lead Type	PB-Free	Moisture Sensitivity Level
WLCSP (2.19 mm x 2.47 mm)	30	BGA Solder	Sn-Ag-Cu	1
VFBGA[b] (3.5 mm x 3.5 mm)	64	BGA Solder	Sn-Ag-Cu	1

a. WLCSP = Wafer Level Chip Scale Package
b. VFBGA = Very Fine Ball Grid Array

Package Thermal Characteristics

The PolarPro 3E solution platform is available for Commercial (-20°C to 85°C Junction) temperature ranges.

Thermal Resistance Equations:

$\theta_{JC} = (T_J - T_C)/P$
$\theta_{JA} = (TJ - TA)/P$
$P_{MAX} = (T_{JMAX} - T_{AMAX})/\theta_{JA}$

Parameter Description:

θ_{JC}: Junction-to-case thermal resistance

θ_{JA}: Junction-to-ambient thermal resistance

T_J: Junction temperature

T_A: Ambient temperature

P: Power dissipated by the device while operating

P_{MAX}: The maximum power dissipation for the device

T_{JMAX}: Maximum junction temperature

T_{AMAX}: Maximum ambient temperature

NOTE: Maximum junction temperature (T_{JMAX}) is 125°C. To calculate the maximum power dissipation for a device package look up θ_{JA} from **Table 41**, pick an appropriate T_{AMAX} and use: $P_{MAX} = (125°C - T_{AMAX})/ \theta_{JA.}$

Table 41: Package Thermal Characteristics

Device	Package Description			Theta-JC (° C/W)	Air Flow (m/sec)	Theta-JA (° C/W)
	Package Code	Package Type	Pin Count			
PolarPro 3E	WDN	WLCSP (2.19 mm x 2.47 mm)	30	5.3	0.0	71.5
					0.5	66.4
					1.0	65.0
					1.5	64.1
	PDN	VFBGA (3.5 mm x 3.5 mm)	64	36.3	0.0	69.9
					0.5	67.6
					1.0	66.7
					1.5	66.1

Reflow Profile

QuickLogic follows IPC/JEDEC J-STD-020 specification for lead-free devices. **Figure 30** shows the Pb-free component preconditioning reflow profile.

Figure 30: Pb-Free Component Preconditioning Reflow Profile

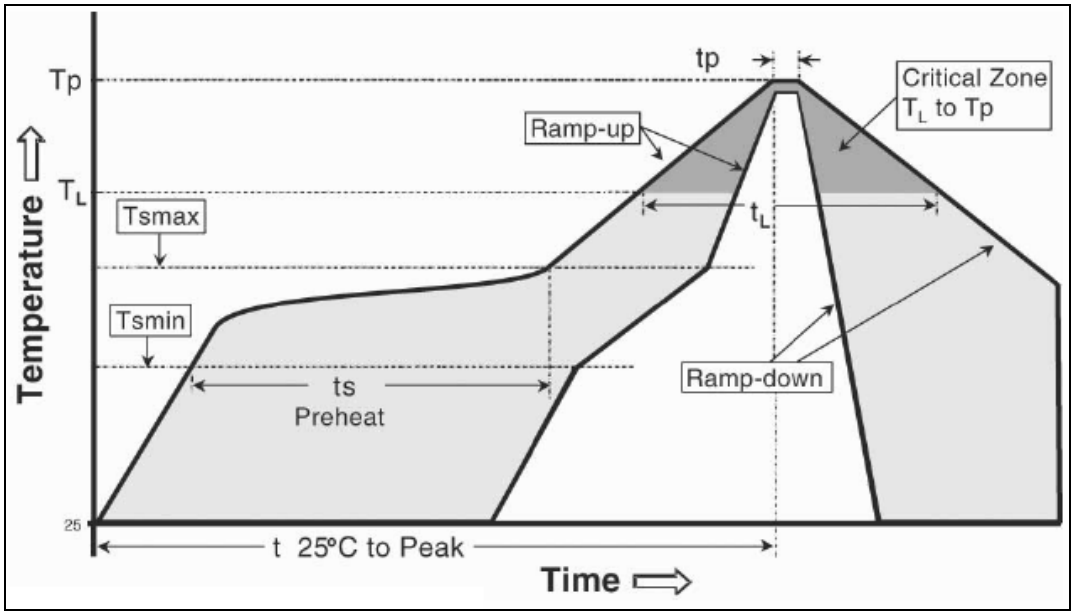


Table 42 shows the Pb-free component preconditioning reflow profile.

Table 42: Pb-Free Component Preconditioning Reflow Profile[a,b]

Profile Feature	Profile Conditions
Average ramp-up rate (Ts_{max}) to Tp)	3° C per sec. max.
Preheat: - Temperature Min (Ts_{min}) - Temperature Max (Ts_{max}) - Time (Ts_{min} to Ts_{max}) (ts)	150°C 200°C 60 sec. to 120 sec.
Time maintained above: - Temperature (T_L) - Time (t_L)	217°C 60 sec. to 150 sec.
Peak Temperature (Tp)	260°C
Time within 5°C of actual Peak Temperature (260°C)	20 sec. to 40 sec.
Ramp-down Rate	6°C per sec. max.
Time 25°C to Peak Temperature	8 min. max.

a. The above conditions are used for component qualifications. This should not be interpreted as the recommended profile for board mounting. Customers should optimize their board mounting reflow profile based on their specific conditions such as board design, solder paste, etc.

b. All temperatures are measured on the package body surface.

Pin Descriptions

The PolarPro 3E – 30-ball pin descriptions are provided in **Table 43**.

Table 43: PolarPro 3E – 30-Ball WLCSP Pin Descriptions

Pin	Direction	Function	Description
Dedicated Pin Descriptions			
CLK_1 - CLK_5/ GPIO(D:A)	I	Global clock network pin Low skew global clock	Capable of being a general purpose I/O, or as a clock. When used as a clock, this pin provides access to a distributed network capable of driving the CLOCK, SET, RESET, all inputs to Logic Cells, READ, and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, and I/O inputs. The letter inside the parenthesis means that the I/O is located in the Bank with that letter.
GPIO(A)	I/O	General Purpose Input/Output pin	The I/O pin is a bi-directional pin, configurable to either an input-only, output-only, or bi-directional pin. Since Bank A is also used by the SPI interface, the I/O voltages of signals on Bank A must match the SPI interface.
GPIO(D:B)	I/O	General Purpose Input/Output pin	The I/O pin is a bi-directional pin, configurable to either an input-only, output-only, or bi-directional pin. The letter inside the parenthesis means that the I/O is located in the Bank with that letter.
VCC	I	Power supply pin	Connect to 1.2V supply.
VCCIO(A)	I	Input voltage tolerance pin	This pin provides the flexibility to interface the device with either a 3.3 V, 2.5 V, or 1.8 V device. VCCIO A is also used by the SPI interface.
VCCIO(E:B)	I	Input voltage tolerance pin	This pin provides the flexibility to interface the device with either a 3.3 V, 2.5 V, or 1.8 V device. The letter inside the parenthesis means that VCCIO is located in the BANK with that letter.
GND	I	Ground pin	Connect to ground
SPI Pin Descriptions			
SPI_RST_N(E)	I	SPI Reset	Reset input (active low). To initiate configuration loading.
CFG_DONE(E)	O	SPI Configuration Done	Configuration done output. Outputs a logic 1 when configuration is successful.
SPI_CS_N(A)	I/O	SPI Chip Select	Selects the SPI mode of operation upon de-assertion of SPI_RST_N. “1” – Master mode “0” – Slave mode
SPI_MISO(A)	I/O	SPI Master Input/Slave Output	Master Input/Slave Output.
SPI_MOSI(A)	I/O	Master Output/Slave Input	Master Output/Slave Input.
SPI_CLK(A)	I/O	SPI Clock	Dual function clock signal. Output in Master mode and input in Slave mode.

Recommended Unused Pin Terminations for PolarPro 3E Devices

All unused, general purpose I/O pins can be tied to their respective VCCIO, GND, weak pull-down resistor, or can be left floating.

The PolarPro 3E – 64-Ball pin descriptions are provided in **Table 44**.

Table 44: PolarPro 3E – 64-Ball VFBGA Pin Descriptions

Pin	Direction	Function	Description
Dedicated Pin Descriptions			
CLK_1 - CLK_5/ GPIO(D:A)	I	Global clock network pin Low skew global clock	Capable of being a general purpose I/O, or as a clock. When used as a clock, this pin provides access to a distributed network capable of driving the CLOCK, SET, RESET, all inputs to Logic Cells, READ, and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, and I/O inputs. The letter inside the parenthesis means that the I/O is located in the Bank with that letter.
GPIO(A)	I/O	General Purpose Input/Output pin	The I/O pin is a bi-directional pin, configurable to either an input-only, output-only, or bi-directional pin. Since Bank A is also used by the SPI interface, the I/O voltages of signals on Bank A must match the SPI interface.
GPIO(D:B)	I/O	General Purpose Input/Output pin	The I/O pin is a bi-directional pin, configurable to either an input-only, output-only, or bi-directional pin. The letter inside the parenthesis means that the I/O is located in the Bank with that letter.
VCC	I	Power supply pin	Connect to 1.2V supply.
VCCIO(A)	I	Input voltage tolerance pin	This pin provides the flexibility to interface the device with either a 3.3 V, 2.5 V, or 1.8 V device. VCCIO A is also used by the SPI interface.
VCCIO(E:B)	I	Input voltage tolerance pin	This pin provides the flexibility to interface the device with either a 3.3 V, 2.5 V, or 1.8 V device. The letter inside the parenthesis means that VCCIO is located in the BANK with that letter.
GND	I	Ground pin	Connect to ground
SPI Pin Descriptions			
SPI_RST_N(E)	I	SPI Reset	Reset input (active low). To initiate configuration loading.
CFG_DONE(E)	O	SPI Configuration Done	Configuration done output. Outputs a logic 1 when configuration is successful.
SPI_CS_N(A)	I/O	SPI Chip Select	Selects the SPI mode of operation upon de-assertion of SPI_RST_N. “1” – Master mode “0” – Slave mode
SPI_MISO(A)	I/O	SPI Master Input/Slave Output	Master Input/Slave Output.
SPI_MOSI(A)	I/O	Master Output/Slave Input	Master Output/Slave Input.
SPI_CLK(A)	I/O	SPI Clock	Dual function clock signal. Output in Master mode and input in Slave mode.

Recommended Unused Pin Terminations for PolarPro 3 Devices

All unused, general purpose I/O pins can be tied to their respective VCCIO, GND, weak pull-down resistor, or can be left floating.

Packaging Pinout Tables

PolarPro 3E – 30-Ball (2.19 mm x 2.47 mm) WLCSP Pinout

Table 45: PolarPro 3E – 30-Ball (2.19 mm x 2.47 mm) WLCSP Pinout

Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	SPI_MOSI/GPIO(A)	B4	GND	D2	VCCIO(C)	E5	GPIO(D)
A2	SPI_MISO/GPIO(A)	B5	VCCIO(E)	D3	VCCIO(D)	F1	GPIO(C)
A3	CLK_5/GPIO(A)	C1	GND	D4[a]	GPIO(D)	F2	CLK_3/GPIO(C)
A4	GND	C2	SPI_CS_N/GPIO(A)	D5[a]	GPIO(D)	F3[b]	CLK_1/GPIO(C)
A5	SPI_CFG_DONE(E)	C3	VCC	E1	GPIO(C)	F4	GPIO(C)
B1	CLK_4/GPIO(A)	C4[a]	GPIO(D)	E2[b]	CLK_2/GPIO(C)	F5[b]	GPIO(D)
B2	VCCIO(A)	C5	SPI_RST_N(E)	E3	GND		
B3	SPI_CLK/GPIO(A)	D1	VCC	E4[b]	GPIO(D)		

a. Pins C4, D4, and D5 are dedicated to dual drive.
b. Pins E2, E4, F3, and F5 are used for pull-ups.

PolarPro 3E – 64-Ball (3.5 mm x 3.5 mm) VFBGA Pinout

Table 46: PolarPro 3E – 64-Ball (3.5 mm x 3.5 mm) VFBGA Pinout

Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	SPI_CFG_DONE(E)	C1	SPI_RST_N(E)	E1	GPIO(D)	G1	GPIO(D)
A2	GPIO(A)	C2	GPIO(D)	E2	GPIO(D)	G2	GPIO(C)
A3	SPI_CS_N/GPIO(A)	C3	GPIO(D)	E3	VCCIO(D)	G3	GPIO(C)
A4	CLK_5/GPIO(A)	C4	GND	E4	GND	G4	VCCIO(C)
A5	CLK_4/GPIO(A)	C5	GND	E5	VCC	G5	CLK_3/GPIO(C)
A6	SPI_MOSI/GPIO(A)	C6	GND	E6	VCC	G6	GPIO(B)
A7	GPIO(A)	C7	GPIO(B)	E7	GPIO(B)	G7	GPIO(B)
A8	GPIO(B)	C8	GPIO(B)	E8	VCCIO(B)	G8	GPIO(B)
B1	VCCIO(E)	D1	GPIO(D)	F1	GPIO(D)	H1	GPIO(D)
B2	GPIO(A)	D2	GPIO(D)	F2	GPIO(C)	H2	GPIO(C)
B3	SPI_CLK/GPIO(A)	D3	GPIO(D)	F3	CLK_1/GPIO(C)	H3	GPIO(C)
B4	VCCIO(A)	D4	GND	F4	GPIO(C)	H4	CLK_2/GPIO(C)
B5	SPI_MISO/GPIO(A)	D5	VCC	F5	GND	H5	GPIO(C)
B6	GPIO(A)	D6	VCC	F6	GND	H6	GPIO(C)
B7	GPIO(A)	D7	GPIO(B)	F7	GPIO(B)	H7	GPIO(C)
B8	GPIO(B)	D8	GPIO(B)	F8	GPIO(B)	H8	GPIO(B)

Power-up Sequencing

Figure 1: Power-Up Sequencing

Power-up sequencing timing will be provided once production silicon characterization is completed.

Package Mechanical Drawings

Figure 31: PolarPro 3E – 30-Ball (2.19 mm x 2.47 mm) WLCSP

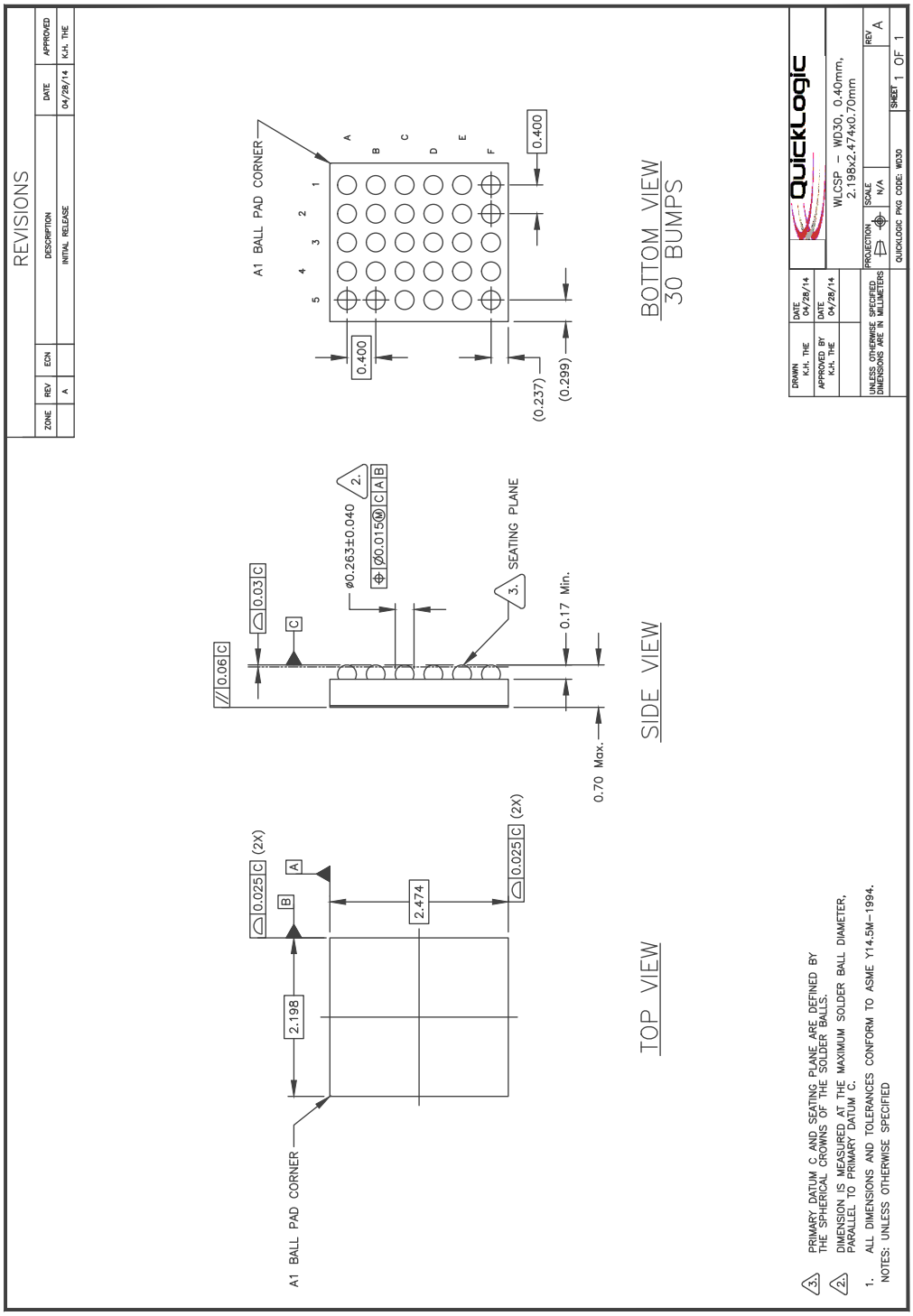
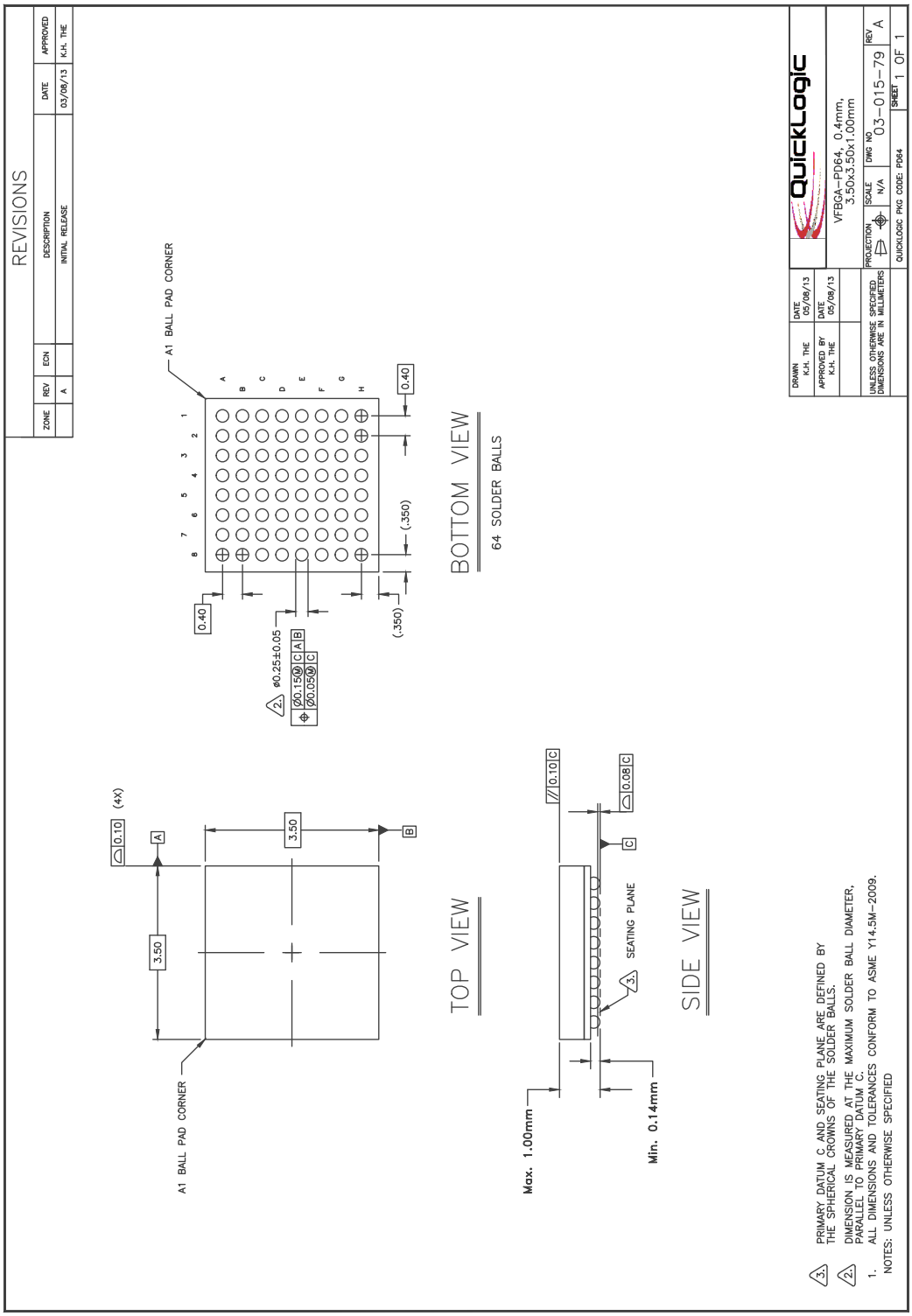


Figure 32: PolarPro 3E – 64-Ball (3.5 mm x 3.5 mm) VFBGA



Reference Schematic

PCB Design Guidelines

Figure 33: VFBGA – PCB Design Guidelines

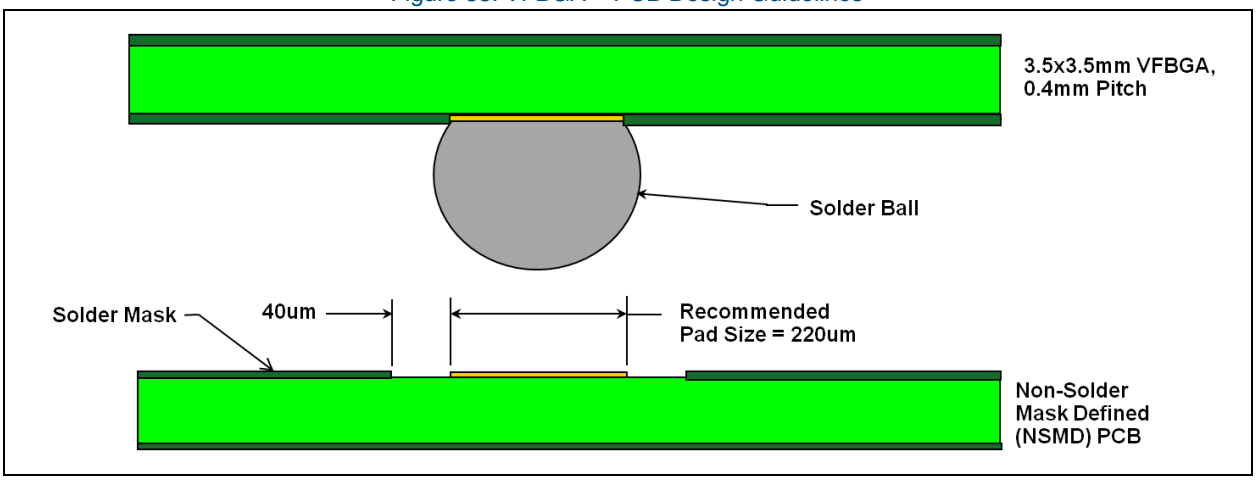
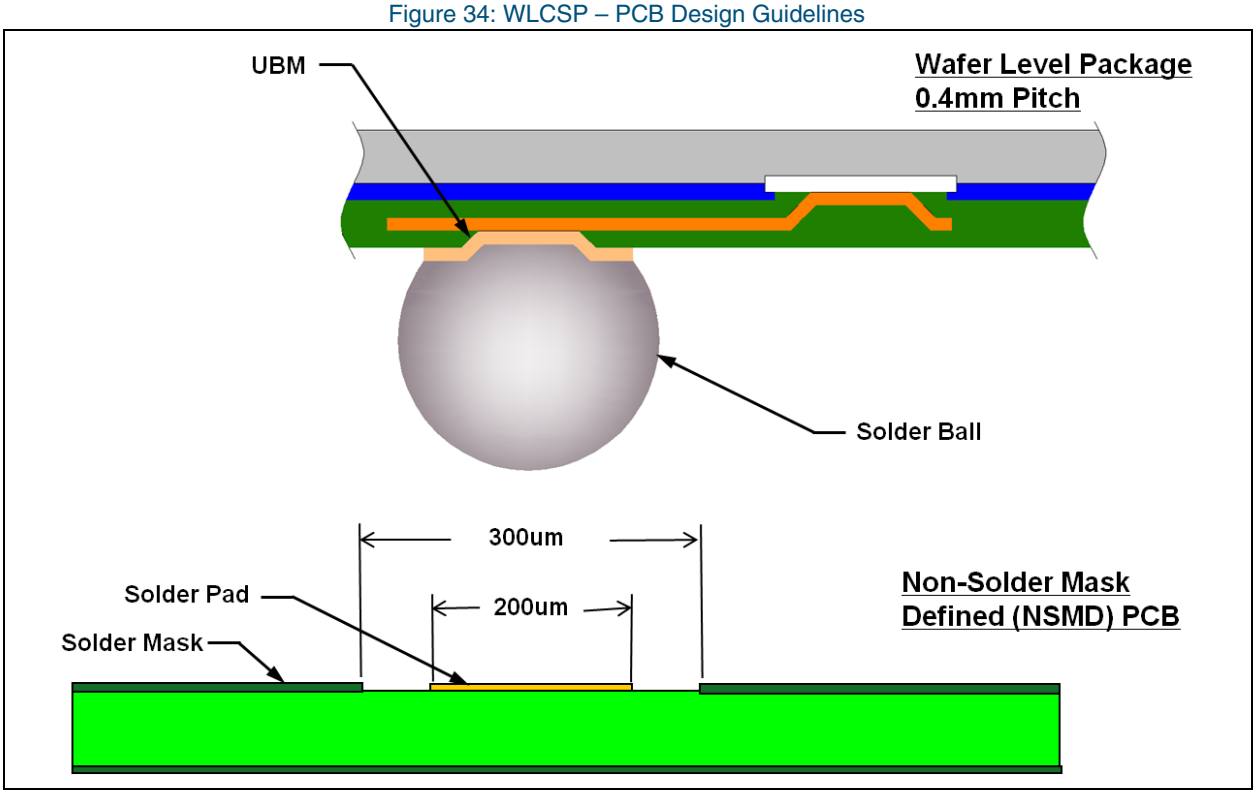


Figure 34: WLCSP – PCB Design Guidelines



PCB Layout Guidelines

When designing a PolarPro 3E PCB, extreme care must be given to the following areas:

- Device interface signals: clock and other data lines that run between devices on the PCB.
- Power going into the device from the connector: the power lines to the PolarPro 3E device must be filtered to pass only low frequency signals of less than 100 kHz. The ground signals must have returned current during data transmission.
- External clock circuit.

Generic Layout Guidelines

The following generic guidelines are from QuickLogic for a board design that contains PolarPro 3E devices. PCB designers should consult internal PCB design rules and recommendations, as well as other device manufacturers, to produce a working PCB.

Important PCB design elements include:

- Type of circuit (analog, digital, etc.)
- Board size
- Number of layers
- Pad stack sizes
- Hole sizes
- Layer thickness
- Board thickness
- External connections
- Mounting holes
- Supply and ground layer thickness
- Component details with specifications

Important design rules are:

- Power distribution and coupling
- Critical signal paths
- IR [Current (I) x Resistance (R)] drops in signal and power traces
- Impedance control
- Pad/land geometries
- Trace width/spacings
- Plated/unplated hole sizes
- Part placement constraints

- Layer assignments and routing constraints
- Heat-removal paths
- Test requirements

Partitioning

The following guidelines are recommended for system partitioning:

- Divide the system into subsystems for placement. The division is used for layout partitioning of circuitries. Group components belonging to a functional block together.
- Isolate sensitive circuits (such as clocks and analog supplies) from noisy sources (such as high transition signals and power regulators).
- Separate analog power supplies from digital power supplies.

Placement

A system with a PolarPro 3E is comprised of a set of interacting elements responding to inputs to produce outputs. Good placement for logical data flow is important to keep the number of layers to a minimum.

The following guidelines are recommended for placement of components:

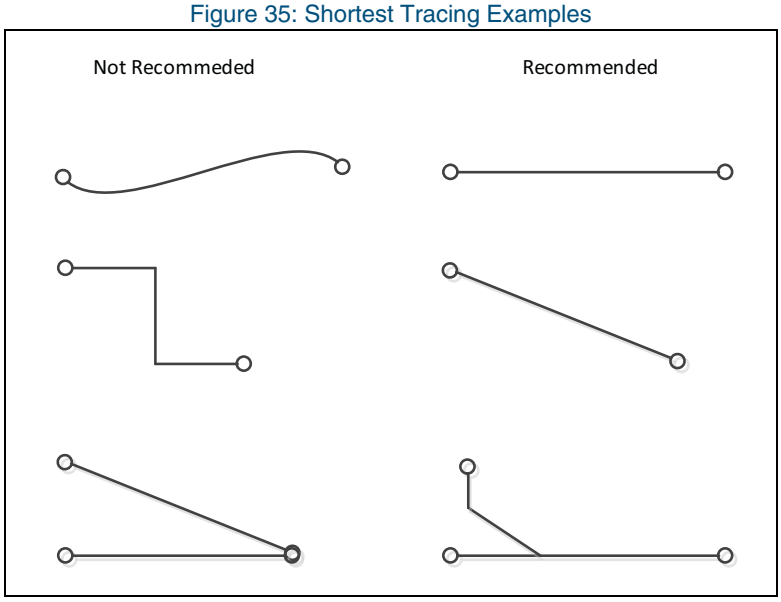
- For highly-sensitive circuits, place the critical components first to produce minimum trace-length.
- For less-critical circuits, arrange the components in the order of the signal flow to minimize the overall connection length.
- For components that have many connecting points, place these components first and group the remaining ones around them.
- For components with a fixed position (such as connectors), place these components first followed by components that are connected to the fixed components.
- Place the larger components (such as main devices) first. Place the smaller components (such as capacitors and resistors) between the larger components.
- Place components in rows or columns for good viewing.
- Place decoupling capacitors as close as possible (preferably adjacent) to the power pins of the device for maximum effectiveness.

Routing

The following guidelines are recommended for routing:

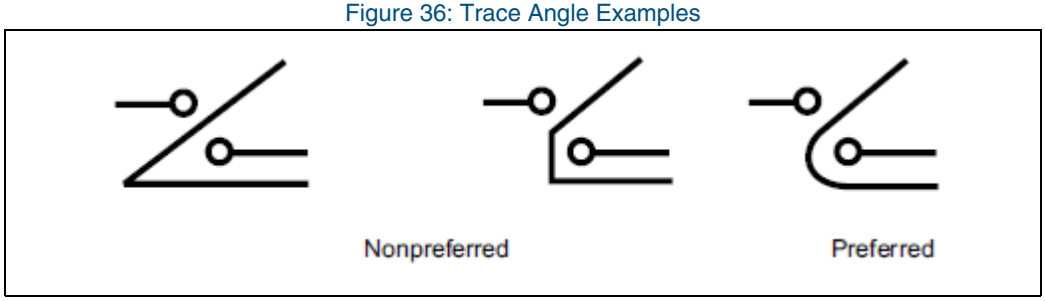
- Select the shortest interconnection length, especially for high frequency circuits (see **Figure 35**).

Figure 35: Shortest Tracing Examples



- Place traces with a minimum angle of 60 degrees (see **Figure 36**).

Figure 36: Trace Angle Examples



- Place parallel traces at the same angle to ensure uniformity, and eliminate the variance in the traces spacing.
- Distribute the spacing equally when one or more traces pass between pads or other conductive areas. To obtain maximum spacing, place traces perpendicular to a narrow passage.
- Distribute traces widely over the available area to avoid issues in manufacturing (i.e., do not space parallel running traces closely).
- Avoid unwanted bunching.
- Match signal impedance for all high-speed signals.
- Ensure that power lines are as thick as possible. Check the current requirements for the line.
- Ensure that the ground traces are always two times wider than the power traces.
- Distribute the routing pattern equally between the various layers of the PCB to achieve uniform plating in the manufacturing process.

- Route adjacent signal layers orthogonally to each other.
- Place ground or power planes to isolate signal layers when possible.
- Route traces directly to a connector pad without line branching to prevent reflections and impedance changes.
- Use curves or two 45° turns to avoid minor line reflections.
- Avoid line-width changes that can affect trace impedance.
- Make pads with soldered signal traces tear-dropped at the pad junction.

Power

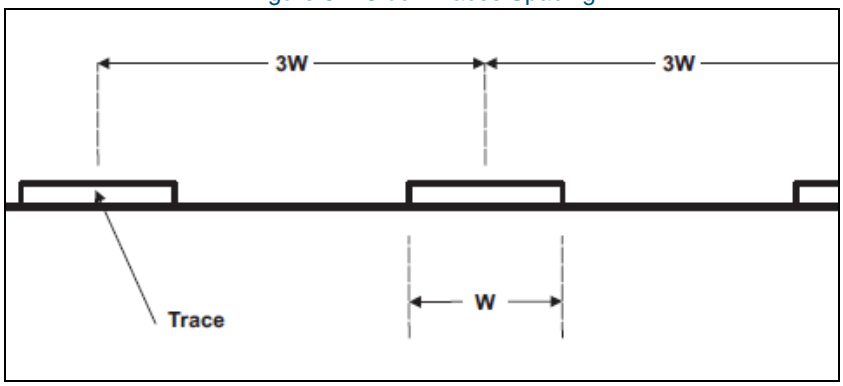
Switching power regulators are noisy and can cause noise-coupling issues if placed close to sensitive areas on the PCB. Keep these circuits away from the sensitive traces, clock circuits and connectors.

Clock Routing

The following guidelines are recommended for clock routing:

- Use series terminator resistors to eliminate reflections. Obtain the final value by looking at the waveform using a high-speed oscilloscope to obtain minimum distortion on the signal.
- Use the 3W spacing rule when routing clock traces from one device to another to minimize cross-talk (see **Figure 37**).

Figure 37: Clock Traces Spacing



- Do not use 90° angles for bending.
- Include guard traces (ground) to surround the clock signal if possible.
- Place clock routing on an internal layer without stubs.

High-Speed Differential Pair

The following guidelines are recommended for high-speed input and output signal layout:

- For low-swing signals (<300 mV), place the device as close to the driving source as possible (such as the flexible printed circuit or processor) to minimize the cross-talk, impedance mismatch, and differential noise pick-up. Keep the total trace-length <4 inches.
- Traces must always be matched lengths.
- Route the pair as close together as possible for noise rejection.
- Trace impedance must be 100 Ohm ± 10% to produce a 50 Ohm ± 10% pair.
- Signals must not have extra components to maintain signal integrity.

Vias

The following guidelines are recommended for via usage:

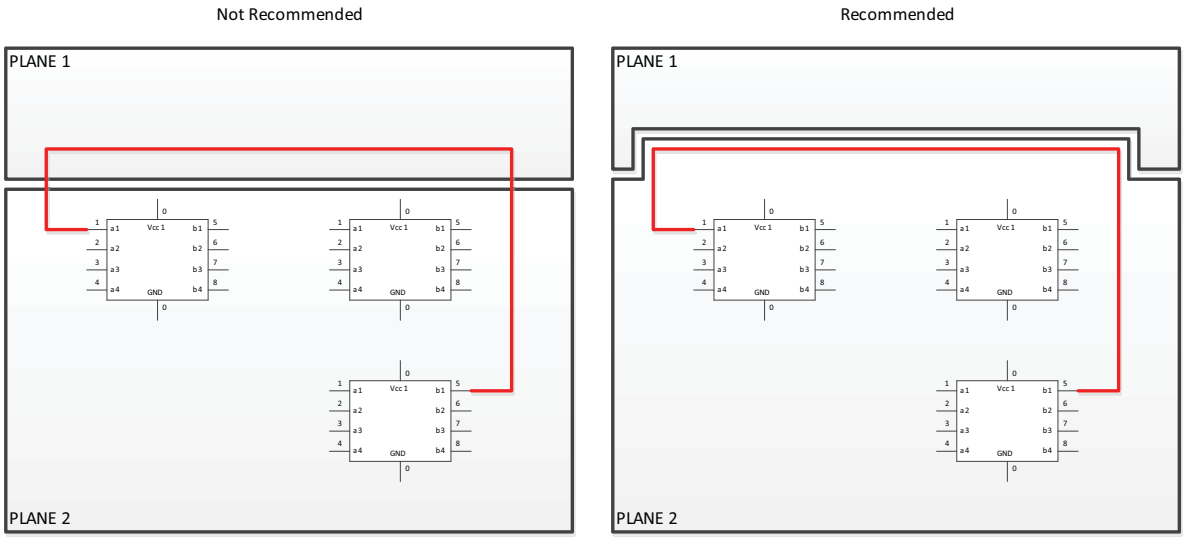
- Increase the clearance around the via to minimize capacitance.
- Minimize the number of vias per signal connection. Each via introduces discontinuities in the signal transmission line and increases the chance to pick up interference from other layers of the PCB.
- Avoid using a through-hole via as a test point if possible.

Isolations

Isolation is referred to as the separation between power and ground planes. The following guidelines are recommended for isolation:

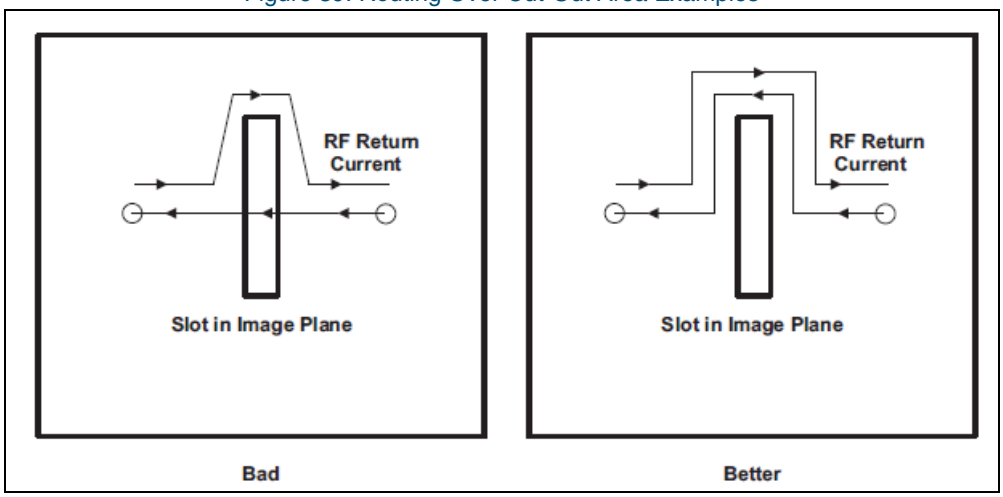
- Isolate between digital and analog power planes.
- Do not route traces across planes (see **Figure 38**). This can cause a broken RF path for the return signal, which can result in severe EMI issues. Route high-speed sensitive signals parallel to solid power or ground planes.

Figure 38: Routing Over Isolation Planes



- Fill unused areas of a layer with copper and connect to ground planes using vias.
- Do not overlap planes between layers. These overlap areas can produce unwanted capacitance that passes RF emissions between the planes.
- Do not route signals over the slot-plane (see **Figure 39**).

Figure 39: Routing Over Cut-Out Area Examples



Electrostatic Discharge (ESD)

The following guidelines are recommended for ESD:

- Provide ESD protection for PCB handling. The typical provision is an ESD strip around the board. The strip must connect to the PCB ground plane.
- Apply ESD protection to all connectors. The ground of the connector body must be connected to the PCB ground plane.

Layout Guidelines Specific to the PolarPro 3E

Critical Signals

The following guidelines are recommended for the layout of critical signals:

- Keep the PolarPro 3E reference clock circuits as close to the device as possible.
- Follow the minimum spacing rules for reset lines from adjacent signals on the same and adjacent layers.
- Keep reset lines away from noisy sources (such as long clock traces, high energy signals and fast transition edges signals).
- Keep interrupt lines away from noisy sources (such as long clock traces, high energy signals and fast transition edges signals).

Vias

Use via-in-pad for the layout of vias and device connections.

GPIOs

The following guidelines are recommended for the layout of GPIOs:

- Keep the number of vias as close to minimum (two) as possible.

Power

The following guidelines are recommended for the layout of power:

- Use the power island or plane as much as possible.
- If using a power trace to connect to the PolarPro 3E power pins, make the trace as wide as possible, and follow current requirements to prevent excessive IR drop.
- Since the number of capacitors for the design is at a minimum, place all of the capacitors as close to the power pins as possible.

Reducing the Number of PCB Layers

The cost-reduction requirements common to PCB design and manufacturing requires the PCB designer to look for a solution to produce PCBs at the lowest cost possible. This section discusses areas that a PCB designer needs to consider when using a PolarPro 3E in the system.

There are several factors that contribute to the cost of a bare PCB:

- Volume: the number of PCBs per run.
- PCB size: the smaller, the less costly.
- PCB material: readily available material is less expensive.
- Number of layers: thickness reduction and quicker manufacturing time.
- PCB shapes: odd shape and slots require more processes.
- Copper size and spacing: the dimension of pads and spacing demand better PCB producing equipment.
- Via: current PCB technology is capable to handle more advanced via types: blind, buried, etc. These require more manufacturing time which translates into a more costly PCB.

Work with the PCB manufacturer to understand the trade-offs between PCB cost and these factors before finalizing PCB specifications.

Device Placement

Placement of devices is critical for good flow to nets routing, thus reducing the number of layers required. The placement must follow the flow of data between components. Critical components must be placed first, followed by support components such capacitors. Less critical components are placed last.

Make sure the device orientation is correct. If the device is in the correct location, but with the wrong orientation, the intended result may not be achieved. Always choose the orientation that has the most signals flowing in the same direction. Crossing signals require multiple layers to complete routing.

Via Technology

While advanced via technologies are more expensive that regular thru-hole via, they can be used to improve layers routing. Use blind via and/or buried via for a design that has constraints on PCB size (thus requiring routing of a signal under the PolarPro 3E). Using via-in-pad for PolarPro 3E pins that need internal layer connections.

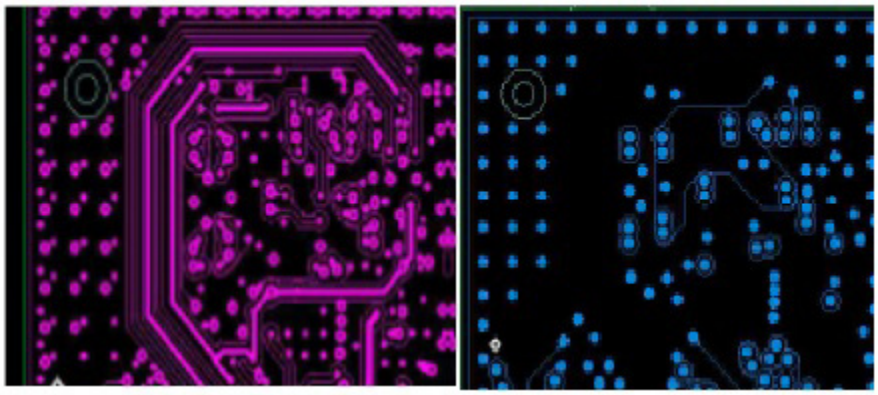
Power and Ground Planes

Dedicated power and ground planes yield the best impedance control and zero IR drop. However, these dedicated planes increases the thickness, and layers count for the PCB.

To reduce the need for a dedicated power plane, use thick traces for power routing. The thickness must meet the current requirements and be as wide as space allows.

To reduce the need for a dedicated ground plane, provide guards around the traces for each layer and fill the rest of the layer with copper (see **Figure 40**). Where possible, provide vias to tie these ground islands on each layer together. While this grounding method is not effective for EMI and trace impedance control, it provides plenty of grounding for the logics.

Figure 40: Fill-In Ground Examples



PCB Size

While increasing the board size can increase the cost of the PCB, this increase can be offset by the reduction of layers. Increasing board size provides additional routing areas and room for parts placement.

Ordering Information

Table 47: Ordering Information

Ordering Number	Package Type[a]
CSSP-CJWDN30-xxxx	30-ball WLCSP 2.19 mm x 2.47 mm, 0.4 mm pitch
CSSP-CJPDN64-xxxx	64-ball VFBGA 3.5 mm x 3.5 mm, 0.4 mm pitch

a. PolarPro 3E devices are only available in lead-free packaging.

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Revision History

Revision	Date	Originator and Comments
1.0	November 2014	Initial production release.
1.1	November 2014	Paul Karazuba and Kathleen Bylsma Minor changes throughout.
1.2	December 2017	Ikuo Nakanishi and Kathleen Bylsma Added 64-ball BGA information.

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