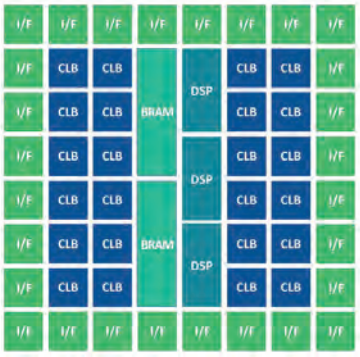
QuickLogic's eFPGA Technology Delivers Post Manufacturing Flexibility

australis

EVALUATE DEFINE GENERATE INTEGRATE INNOVATE

QuickLogic's Australis™ IP Generator enables quick delivery of a customized eFPGA IP core tailored to your requirement.

The Australis IP Generator flow uses a standard cell ASIC flow to automate the creation of the eFPGA IP. It enables delivery of customized eFPGA IP for a multitude of use cases, such as addressing changing market conditions, supporting new standards, offloading AI/ML workloads, and creating product variants.



eFPGA Architecture

Australis IP Generator: Delivers customized eFPGA IP blocks in weeks, not months.

Customization – eFPGA IP can be generated/customized to any foundry/process technology within days for a process we already support and within a quarter for new process technologies.

Fast time-to-market – Australis does not use fixed arrays, so you have complete freedom to design your core the way you want.

Flexibility to meet your SoC design requirements – With Australis, you can specify the number of DSP, LUT, and BRAM columns, as well as the specific placement of these columns. You can also define the size of the X/Y array.

Cost Effective – Our automated approach to core customization significantly reduces costs and time.

Foundry Partners

GlobalFoundries™ SAMSUNG skywater

SMIC tsmc UMC

Learn more about Australis

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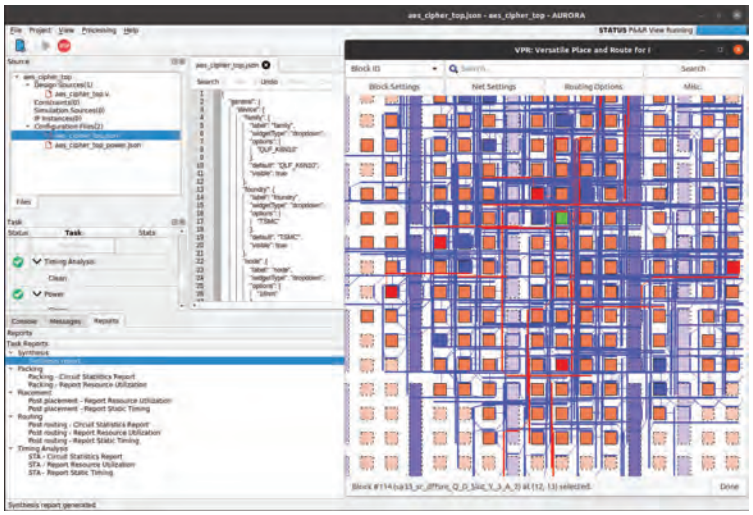
aurora

Aurora™ FPGA User Tools

Scalability • Longevity • Full Code Transparency

Aurora Empowers eFPGA Designers with Greater Transparency and Control

Aurora 2.1 is a fully open-source development tool suite for eFPGA designers. It supports all major HDLs, including Verilog, System Verilog, and VHDL. It is based on open-source synthesis (Yosys), Versatile Place and Route (VPR), and bitstream generation (OpenFPGA) software. The fully integrated suite of tools enables eFPGA designers to go from RTL-to-bitstream for QuickLogic's eFPGA IP.



Aurora User Tools

Simplified Evaluation – Supports quick and easy evaluation of eFPGA technology for SoC applications.

Architectural Trade-Offs – Let's you fine-tune the amount of logic (LUTs), BRAM, and DSP blocks in your eFPGA IP to meet your specific requirements.

Inspectability – Open-source based Aurora promotes transparency; the code is easily inspectable and can be continuously improved by the development community.

Future-Proof – Aurora is built using readily available open-source components that the broader community is actively improving upon, ensuring that users have access to the latest tools.

Learn more about Aurora

QuickLogic

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